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# A novel Sigma–Delta based parallel analogue-to-residue converter

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An important step in the residue number system (RNS) based signal processing is the conversion of signal into residue domain. Many implementations of this conversion have been proposed for various goals, and one of the implementations is by a direct conversion from an analogue input. A novel approach for analogue-to-residue conversion is proposed in this research using the most popular Sigma–Delta analogue-to-digital converter (SD-ADC). In this approach, the front end is the same as in traditional SD-ADC that uses Sigma–Delta ($\Sigma\Delta$) modulator with appropriate dynamic range, but the filtering is done by a filter implemented using RNS arithmetic. Hence, the natural output of the filter is an RNS representation of the input signal. The resolution, conversion speed, hardware complexity and cost of implementation of the proposed $\Sigma\Delta$ based analogue-to-residue converter are compared with the existing analogue-to-residue converters based on Nyquist rate ADCs.

**Keywords:** analogue-to-residue converter; Sigma–Delta modulator; decimation filter; residue number system; performance evaluation



## 1. Introduction

Most of the real time digital signal processing (DSP) algorithms are based on intensive multiplication and addition operations. In real time systems digital convolution, finite impulse response (FIR) filtering, discrete Fourier transforms (DFT) and similar computations are at high sampling rate on long word lengths. The carry propagating multipliers and adders in binary number systems become the bottle-neck for high sampling rate computations. The use of residue number system (RNS) draws a great deal of interest in such computationally intensive DSP applications as it significantly speeds up multiply and accumulate (MAC) operations (Parhami 2000). Also, for higher orders and large dynamic range, the filters implemented in RNS are significantly smaller than filters implemented in the traditional two's complement number system (TCS). A design space exploration is carried out in Cardarilli, Ret, Nannarelli and Re (2007) to identify the trade offs between filters realised in TCS and RNS in terms of filter order, dynamic range, clock frequency and area. The non-positional nature of RNS makes it suitable for fault-tolerant architectures. The error detection and correction properties are obtained by introducing few redundant moduli that are relatively prime to the non-redundant moduli. By including '$k$' redundant moduli, it is possible to detect $k$ errors and to correct $\lfloor k/2 \rfloor$ errors (Soderstrand,

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Jenkins, Jullien and Taylor 1986). In Redundant Residue Number System (RRNS) the representation range is divided into two intervals: the legitimate range and the illegitimate range. An error in a single module is detected if the number belongs to the illegitimate range. As there is a unique error pattern, error correction can be done with the help of a look-up table (Cosentino 1988; Preethy, Radhakrishnan and Omondi 2001.). Another error detection and correction technique based on the selection of a particular subset of the legitimate range of the RNS representation is presented in Pontarelliz, Cardarilliy, Rey and Salsanoy (2008). It is characterised by the property that each element of the subset is a multiple of a number $m$ with the constraint that $m > m_i$, where $m_i$ is an element of the set of moduli used in the RNS representation. The RRNS codes exhibit identical distance properties to Reed–Solomon codes, and offer greater flexibility. The performance of RRNS is studied over Additive White Gaussian Noise (AWGN) and Rayleigh channels (Liew, Yang and Hanzo 2006). The RNS also finds application in cryptographic systems which require multiplication of very large numbers.

RNS is a non-weighted number system defined by a set of '$r$' relatively prime integers $(m_1, m_2, \ldots, m_r)$ which are called the moduli. The dynamic range '$M$' of the number system is given by the product of the moduli, $M = \prod_{i=1}^{r} m_i$. Any integer '$X$' in the interval of $[0, M-1]$ is represented in RNS as a set of '$r$' residues $(x_1, x_2, \ldots, x_r)$, where $x_i = X \bmod m_i$ is the least non-negative remainder on dividing '$X$' by $m_i$. In RNS, arithmetic operations are computed by the formula: $(x_1, x_2, \ldots, x_r) \otimes (y_1, y_2, \ldots, y_r) = (z_1, z_2, \ldots, z_r)$, where $z_i = |x_i \otimes y_i|_{m_i}$ and $\otimes$ denotes one of the operations of addition, subtraction or multiplication. Thus arithmetic operations on residues can be performed in parallel without any carry propagation among the residue digits. This leads to a significant speed up of MAC operations in RNS domain. However, before performing any operation on residues the number is converted from binary to residue by performing modulo operations with respect to each modulus in the moduli set. The process of translating a binary integer '$X$' to the residue representation $(x_1, x_2, \ldots, x_r)$ with respect to a relatively prime moduli set $(m_1, m_2, \ldots, m_r)$ is called forward conversion. The analogue-to-residue conversion usually involves two steps. The analogue signal is first converted to digital signal by analogue-to-digital (A/D) converter, then to residue form by a binary-to-residue converter. Getting back to the weighted representation of '$X$' from a given residue representation is referred to as reverse conversion. The forward and reverse conversion circuitries are complex for a general moduli set and limits the applications of RNS.

Many researchers have explored efficient methods for forward and reverse conversions. The direct conversion of analogue signal to residue form using an analogue-to-residue (A/R) converter is available in literature. The direct analogue-to-residue conversion proposed in Mandyam and Stouraitis (1990) uses a flash A/D converter, PLA, latches, code converter, buffers and XOR gates. An $n$-bit converter requires $2^n - 1$ comparators and $2^n$ resistors. Such A/R converters with high resolution are impractical to construct as the number of elements grows exponentially with resolution '$n$'. The design of a direct A/R converter using two stages of successive approximation A/D converters, a few modulo adders and a small look-up table (LUT) is presented in Radhakrishnan and Preethy (1999). Here, the successive approximation A/D converter of the first stage is modified by replacing the comparator with a difference amplifier. A weighting factor '$m_r$', equal to the value of the largest modulus, is applied to the D/A converter output and is fed back to this difference amplifier. The sampled analogue input voltage '$X$' is applied to the input of difference amplifier. The

size of register in the first stage is $k = \lceil \log_2 \left(\frac{M-1}{m_r}\right) \rceil$ bits. The output of the difference amplifier is $X - R \times m_r$, where '$R$' is the value stored in the register. When the first stage stops conversion, the output of the difference amplifier is the voltage equivalent of $x_r = X \bmod m_r$. This residue value '$x_r$' is converted to digital output using the second stage successive approximation A/D converter. The output register size of this converter is $l = \lceil \log_2 m_r \rceil$ bits. The remaining $(r-1)$ residues are generated from the register content '$R$' of the first stage A/D converter and the output register content '$x_r$' of the second stage A/D converter using small ROM LUTs and a few modulo adders. The total conversion time for this A/R converter is approximately $k + l + 2$ clock cycles. An iterative flash A/R converter is presented in Radhakrishnan and Preethy (1998), which uses the principle of subranging to reduce the hardware complexity of flash A/D converters. Here, the first stage flash converter is used iteratively to find the quotient of '$X$' with respect to the largest moduli, $m_r$. The second stage flash A/D converter converts the analogue voltage equivalent to the residue '$x_r$' into binary form. The conversion time for generating residue '$x_r$' is the sum of conversion times in both the flash converter stages. The generation of remaining residues requires additional delay. An analogue-to-residue converter based on the interpretation of properties of RNS as a measurement tool is proposed in Lojacono (2004). It uses a two stage flash-like subranging architecture and a cascade of resistors for realising the voltage scales. A set of comparators for each cascade of resistors produces a thermometer code-like output. This output is used to drive an analogue multiplexer, which selects the proper voltages to be compared in determining the residue. The residues in thermometer code from the comparators are finally encoded in binary form. Similarly, residue-to-analogue converters that convert RNS numbers to equivalent analogue signals are used to reduce the reverse conversion complexity (Bernardson 1986; Lewis, Mellott, Taylot 2004).

A method to enhance the bandwidth efficiency of a multicarrier code division multiple access (MC-CDMA) system by combining RNS representation, PSK/QAM modulation and orthogonal modulation is presented in Madhukumar, Chin and Premkumar (2000) and Madhukumar and Chin (2002). The bandwidth efficiency of an MC-CDMA system can be improved by increasing the number of bits per symbol. The information symbols are represented in RNS to increase the number of bits without increasing the number of parallel channels. This in turn improves the bandwidth efficiency. The residue channels are independently interleaved frame-wise in a systematic fashion such that the individual residue channel belonging to the same modulus is not repeated in the interleaved symbol. These residues are then mapped to an orthogonal sequence, multiplexed and scrambled. This data is modulated in baseband by inverse discrete Fourier transform (IDFT) and transmitted through different subcarriers after guard interval insertion and frequency-up conversion. Orthogonal sequences corresponding to all residues can be transmitted through the same subcarrier without affecting the system performance. This can achieve higher data rate in a multicarrier system. At the receiver after proper synchronisation, the guard interval which is appended to avoid inter symbol and inter carrier interference is removed from the received data packet. The subcarrier components are coherently detected with DFT, and are passed through a bank of subreceivers which are dedicated for each residue channel. The residue digits are finally converted into binary form. The performance evaluation of an RNS-based parallel communication scheme using orthogonal signalling with ratio static test over AWGN channel and multipath fading channel is demonstrated by Yang and Hanzo (2002a,b).

This article proposes a parallel analogue-to-residue converter as a supporting block for the RNS-based MC-CDMA transmitter. The proposed A/R converter is based on a Sigma–Delta (ΣΔ) A/D converter. The main motivations for using ΣΔ based architecture are the following:

- As most of the circuitry in ΣΔ converters is digital, the performance will not drift significantly with time and temperature.
- They do not require external sample and hold circuit because of the high input sampling rate.
- The devices are inherently self-sampling and tracking.
- The background noise level which determines the signal-to-noise ratio (SNR) is independent of input signal level.

The rest of the article is organised as follows: Section 2 describes the architecture of a ΣΔ based A/R converter for various resolutions. Section 3 presents the simulation results and performance comparison with existing A/R converters. Section 4 gives the conclusion.



## 2. Parallel analogue-to-residue converter architecture

The proposed A/R converter architecture based on a ΣΔ based modulator is shown in Figure 1. The analogue input is sampled at an oversampling ratio (OSR) much greater than Nyquist rate. The order of the modulator '*L*', the OSR '*M*' and the number of quantiser bits '*B*' are selected to meet the dynamic range requirements for various resolutions. The binary bits from the ΣΔ modulator are given to the following RNS-based decimation filter. The residue digits are generated in parallel at the decimator outputs.

### *2.1. Sigma–Delta modulator*

A ΣΔ modulator trades resolution in time for resolution in amplitude. Oversampling and noise-shaping are the two key techniques on which the modulator relies. Oversampling reduces the baseband quantisation noise, and noise-shaping moves quantisation noise from the baseband to higher out-of-band frequencies. Hence the ΣΔ modulator is also referred to as a ΣΔ noise shaper. The oversampling and noise shaping techniques are combined to achieve superior resolution with relaxed requirements on analogue hardware compared with Nyquist rate A/D converters (Norsworthy, Schreier and Temes 1997). A simple first-order modulator consists of an integrator and a coarse quantiser placed in a feedback loop. The quantiser in the A/D block can be realised as either a one-bit comparator or a multi-bit quantiser.

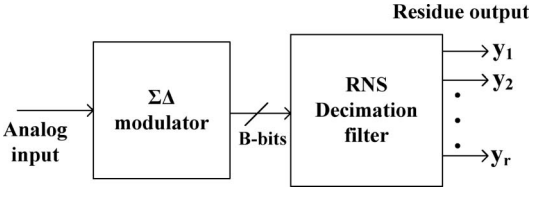


Figure 1. ΣΔ based parallel A/R converter.

The structure is known as an interpolative structure, as the input is fed to the quantiser via an integrator. The feedback of the output, which is subtracted from the input, forces the average value of the quantised output signal to track the input. Any long-term difference between them accumulates within the integrator, and corrects itself eventually.

Single loop and multistage noise shaping (MASH) topologies are two different approaches for implementing ΣΔ modulators. Single loop structures with a higher-order noise transfer function combined with multi-bit feedback can achieve a higher dynamic range with low OSR. But linearity and resolution of the overall ΣΔ modulator are limited by the precision of the multi-bit digital-to-analogue converter (DAC). An alternate way of implementing higher-order ΣΔ modulators is to cascade multiple lower order stages such that each stage processes the quantisation noise of the previous stage. In cascaded or MASH topology, the outputs of each individual stage go to digital error cancellation logic where the quantisation noise of all stages except that of the last one is removed. The quantisation noise of the remaining stage is filtered by the noise transfer function $(1-z^{-1})^L$, where $L$ is the modulator order of the overall ΣΔ modulator. A fourth order ΣΔ modulator can be implemented using two second order stages as shown in Figure 2. The main advantage of MASH architecture is the high degree of noise shaping without any stability problems. However, cascaded modulators require very good matching between analogue and digital processing paths.

Broadband operations require low oversampling ratios because the achievable clock frequency is constrained by the process technology that limits the resolution. Several techniques have been introduced for increasing the resolution of ΣΔ modulators with low oversampling ratios. These are based on increasing the order $L$ and quantiser bits $B$. An approach to achieve higher order noise shaping is to use cascade of multi-bit feed-forward topology. It is a low distortion swing suppression topology suitable for wideband applications with low oversampling ratios (Jose, Mathew, Mythili and Pradhan 2007). Another approach suitable for broadband and high resolution application is presented based on residue averaging technique (Ren

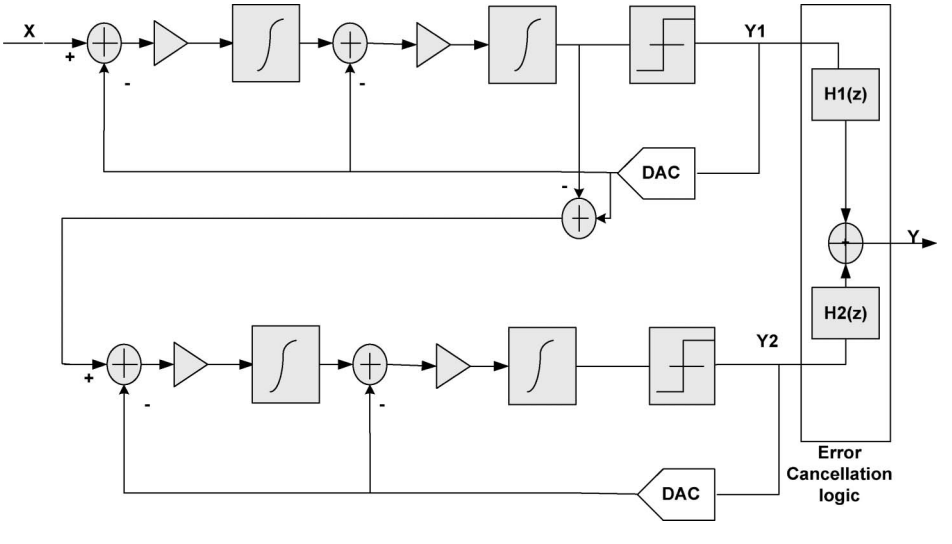


Figure 2. A 2-2 cascaded MASH architecture.

and Siferd 2008). In this method, a Sinc filter residue averaging technique is used that combines the most significant bits of the first stage with the second stage output. This mitigates the effect of DAC non-linearity, component mismatch, etc.

### 2.2. *RNS-based decimation filter*

The oversampling converters relax the requirements placed on analogue circuitry at the expense of more complicated digital circuitry. This trade-off becomes more desirable for modern submicron technologies with low power supplies because the complicated high speed digital circuitry is more easily realisable in a lesser area. But the realisation of high resolution analogue circuitry is complicated by low-power supply voltages and poor transistor output impedance. The decimation filter consists of a lowpass filter and a downsampler. The digital decimation filter serves two purposes. It acts as an antialiasing filter that removes the unwanted noise above the Nyquist band seen in the analogue input spectrum to the ΣΔ modulator. So, it avoids aliasing into the baseband by the decimation process. The decimation filter also removes the out-of-band quantisation noise produced by the ΣΔ modulator. Upon filtering, the output is resampled at the Nyquist rate. A strict linear phase characteristic is required for most digital audio data converters. Hence, symmetric FIR filters are widely used for decimation filter implementations.

The decimation filter receives the output of the ΣΔ modulator as its input. The decimation filter operates in the RNS domain defined by a proper moduli set that provides sufficient dynamic range avoiding overflow. The moduli set consists of relatively prime integers and selected in such a way that the number of bits for representing each modulus is greater than the maximum number of bits from the modulator. This eliminates the need for a forward converter and the output of the modulator '$b$' is directly mapped into the residue domain $(x_1, x_2, \ldots, x_r)$, by a simple encoding as in Equation (1).

$$\begin{aligned} &x_i = b, \forall i \text{ if } b \text{ is positive, and,} \\ &x_i = m_i - |b|, \text{ for } i = 1, 2, \ldots, r \text{ if } b \text{ is negative} \end{aligned} \tag{1}$$

The RNS-based decimation filter is shown in Figure 3, where the MAC operations are performed in the RNS domain. The structure of a particular modulo filter channel based on modulus '$m_i$' is shown in Figure 4, where $\otimes$ and $\oplus$ represent modulo multiplication and modulo addition, respectively. The filter coefficients are

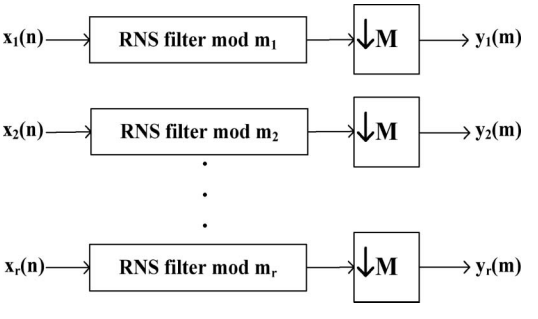


Figure 3. RNS based decimation filter.

directly represented in residue form. Modulo multiplication is implemented with a LUT for faster multiplication, and the size of the LUT is small as the operation is in the residue domain with one of the operands constant. The modulo adder receives the residue digits and performs usual binary addition, followed by modulo correction. The downsampler in each channel resamples the output at Nyquist rate. Here all the residues are generated in parallel at the filter outputs.

## 3. Simulation results and performance evaluation

The proposed parallel A/R converter is simulated for various resolutions. The ΣΔ modulator complexity for an A/R converter with a particular resolution is decided based on the dynamic range (DR) requirement. The dynamic range in dB of an A/D converter with $n$-bit resolution is given in Equation (2). The theoretical DR for a ΣΔ modulator with order '$L$', oversampling ratio '$M$' and number of quantiser bits '$B$' is given in Equation (3). Using Equations (2) and (3), the required modulator order, oversampling ratio and the number of quantiser bits are calculated for a given resolution.

$$\mathrm{DR} = 6.02 \times n + 1.76 \tag{2}$$

$$\mathrm{DR} = \frac{3}{2}\frac{2L+1}{\pi^{2L}} M^{2L+1}(2^B - 1)^2 \tag{3}$$

### 3.1. *Sigma–Delta modulator complexity*

The ΣΔ modulator complexity for A/R converter with various resolutions is shown in Table 1. The A/R converter with 12-bit resolution requires a dynamic range of 74 dB as given by Equation (2). To meet the DR requirement, a fourth order ΣΔ modulator with a 2-bit quantiser and an OSR of 16 is selected using Equation (3). The simulations are performed using the MATLAB® Simulink models. The RNS

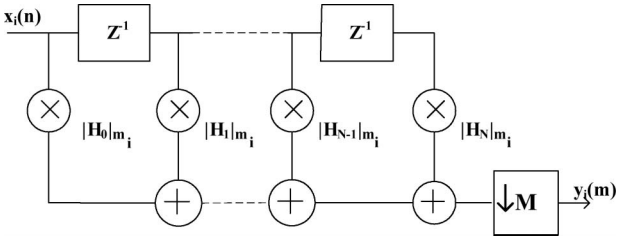


Figure 4. *i*th modulo filter channel.

Table 1. Sigma-delta modulator complexity for A/R converters with various resolutions.

| Resolution (No. of bits) | Sigma–Delta modulator complexity | | | RNS moduli |
|---|---|---|---|---|
| | OSR ($M$) | Order ($L$) | Quantiser bits ($B$) | |
| 12 | 16 | 4 | 2 | [16 19 23] |
| 14 | 16 | 4 | 3 | [17 31 32] |
| 16 | 16 | 5 | 4 | [17 19 31 32] |
| 20 | 32 | 5 | 4 | [17 19 21 31 32] |

moduli set is chosen to provide sufficient dynamic range for the RNS. The Simulink model of a fourth order modulator realised as a 2-2 cascaded MASH architecture as shown in Figure 5.

The fourth order modulator is realised by cascading two second order stages. The first stage in Figure 5 is a second order modulator with a single-bit quantiser. The output of first stage $Y_1(z)$ is given in Equation (4), where $X(z)$ represents the input, and $Q_1(z)$ represents the quantisation noise. The second stage is another second order filter with a two-bit quantiser and receives the quantisation noise of the first stage as the input. The output of second stage $Y_2(z)$ is given by (5), where $Q_2(z)$ represents the quantisation noise of the second stage. The scaling coefficients $g_1$ and $g_2$ of the first stage, and $s_1$ and $s_2$ of the second stage, are optimised to maximise the dynamic range.

$$Y_1(z) = z^{-2}X(z) + (1 - z^{-1})^2 Q_1(z) \tag{4}$$

$$Y_2(z) = z^{-2}Q_1(z) + (1 - z^{-1})^2 Q_2(z) \tag{5}$$

The overall output of the modulator is obtained by combining the output of each stage through error cancellation logic with transfer functions $H_1(z)$ and $H_2(z)$ given by Equations (6) and (7).

$$H_1(z) = z^{-2} \tag{6}$$

$$H_2(z) = (1 - z^{-1})^2 \tag{7}$$

The transfer functions of error cancellation logic are selected such that it cancels the quantisation noise of first stage and produces the final output $Y(z)$ as given in Equation (8).

$$Y(z) = z^{-4}X(z) + (1 - z^{-1})^4 Q_2(z) \tag{8}$$

The simulation result shows a DR of 77.9 dB with a 2-2 cascaded MASH topology for the modulator. The power spectral density (PSD) plot of the output from modulator is shown in Figure 6.

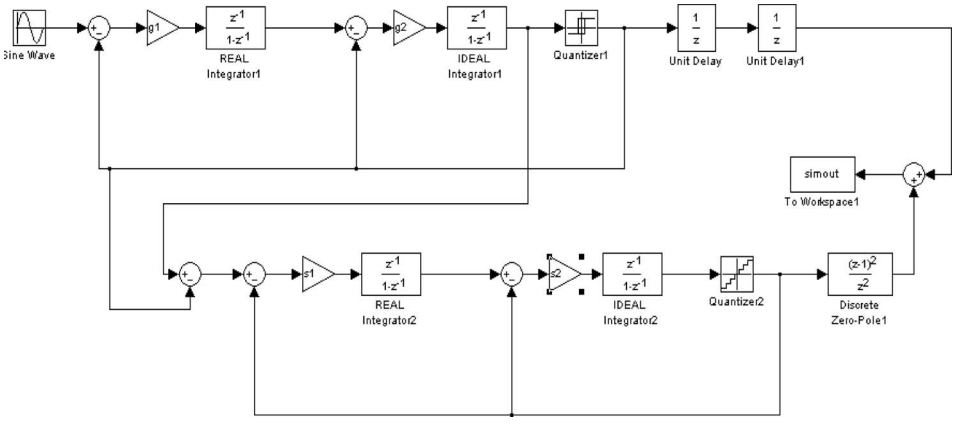


Figure 5. Simulink model for 2-2 cascaded MASH architecture.

### 3.2. *Decimation filter complexity*

The 2-bit output from the ΣΔ modulator is given to the RNS-based decimation filter. The moduli set (16, 19, 23) gives a dynamic range of more than 12-bits for the RNS. The A/R converter is designed to operate in the voice band with 20 kHz bandwidth. The decimation filter is designed to provide 40 dB attenuation in the stopband. The output signal spectrum obtained after digital low-pass filtering in the decimator for an input signal at 5 kHz is shown in Figure 6. The output spectrum at Nyquist rate obtained after downsampling is shown in Figure 7.

The complexities of digital decimation filters for A/R converters with various resolutions in terms of filter order, implementation area and critical path delay are given in Table 2. The Remez-Parks-McClellan optimal equiripple FIR filter is chosen for the implementation. The hardware synthesis is done with the logic synthesis tool *Leonardo Spectrum* from Mentor Graphics Corporation, using the ASIC library. The critical path delay and area for each filter is normalised with respect to a full adder (FA) critical path delay of 0.45 ns and area of 38 $\mu m^2$.

The A/R converters based on Nyquist rate A/D converters are suitable for data conversions in systems where the conversion process is constrained by bandwidth limitations imposed by the technology in which the converter is implemented. Oversampling A/D converters trade resolution in time for resolution in amplitude in order to ease the demands on the precision with which the signal is to be quantised. The ΣΔ based A/R converter is well suited for applications where high resolution is

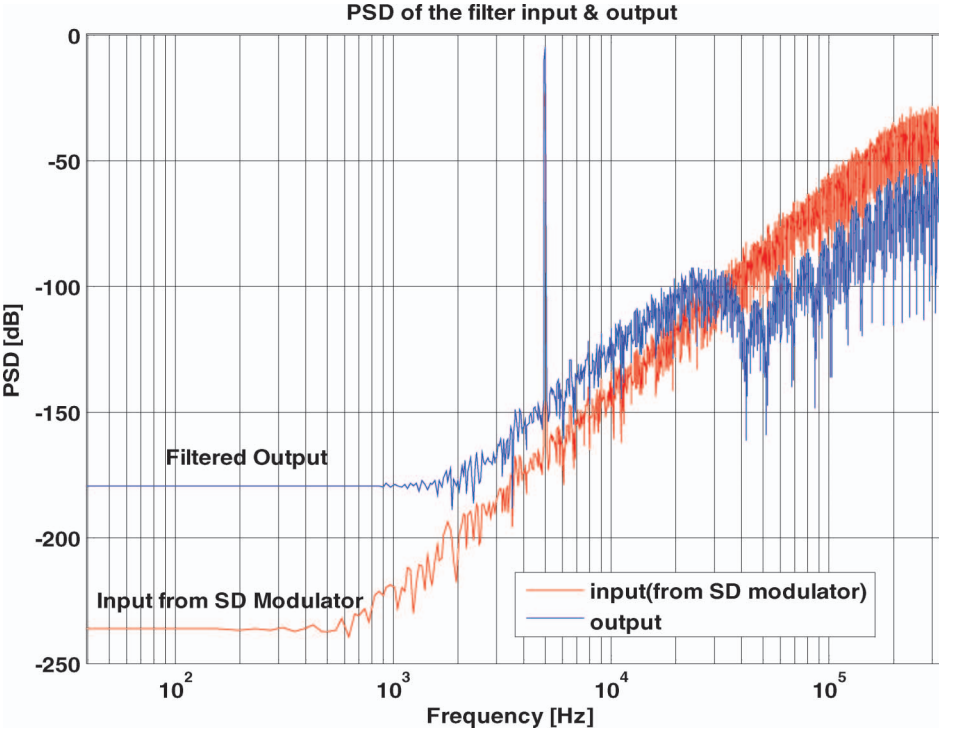


Figure 6. Power spectral density (PSD) plot for filter input and output.

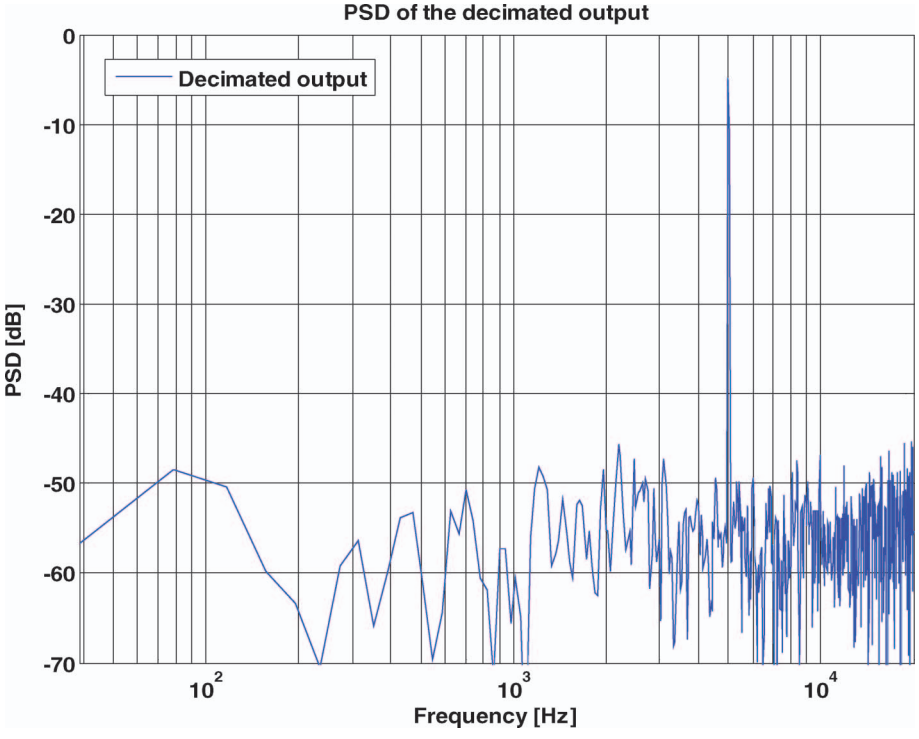


Figure 7. PSD plot for decimation filter output at Nyquist rate.

Table 2. Decimation filter complexities for A/R converters with various resolutions.

| Resolution (bits) | Filter order | RNS moduli | Filter complexity | |
|---|---|---|---|---|
| | | | Area | Delay |
| 12 | 34 | [16 19 23] | 1421.9 | 37.17 |
| 14 | 34 | [17 31 32] | 1271.02 | 37.42 |
| 16 | 34 | [17 19 31 32] | 1865.12 | 37.42 |
| 20 | 68 | [17 19 21 31 32] | 4939 | 43.28 |

needed and the signal bandwidth is much less than the bandwidth limitations imposed by the implementation technology. Nyquist rate A/R converters are practically implemented only up to 10–12 bits of resolution due to component matching and circuit non-idealities. The ΣΔ modulator does not require stringent component matching, and hence ΣΔ based A/R converters with high resolutions of up to 20 bits are practically realisable. The analogue part of a ΣΔ based A/R converter is relatively simple and a low-cost implementation is possible, unlike the Nyquist rate counterparts. This is due to the relaxed requirements for analogue circuitry at the expense of more complicated digital circuitry. This is desirable for modern VLSI technologies with low-power supplies. The complicated, high speed digital circuitry is more realisable in a lesser area than the realisation of high resolution analogue part. The flash A/R converter (Mandyam and Stouraitis 1990) operates at the maximum conversion speed of single clock pulse, but the area

Table 3. Performance comparison of A/R converters.

| Feature | Flash A/R converter (Mandyam and Stouraitis) | SAR-based A/R converter (Radhakrishnan and Preethy 1999) | Iterative flash A/R converter (Radhakrishnan and Preethy 1998) | Two-stage flash-like subranging A/R converter ((Lojacono 2004)) | Proposed Sigma–Delta based A/R converter |
|---|---|---|---|---|---|
| Resolution | 8–10 bits | 10–12 bits | 10–12 bits | 10–12 bits | Up to 20 bits |
| Conversion speed | 1 clock cycle | $(k + l + 2)$ clock cycles | $(p + 1)$ clock cycle | 1 clock cycle | 1 clock cycle |
| Hardware complexity | Highest | Low | Medium | High | Medium |
| Cost of implementation | Highest | Medium | Medium | High | Low |

complexity increases exponentially with resolution. The successive approximation based A/R converter (Radhakrishnan and Preethy 1999) has low area requirement but the conversion speed is $k + l + 2$ clock cycles, where '$k$' and '$l$' are the register size of the first and second stages. The iterative flash A/R converter (Radhakrishnan and Preethy 1998) is a compromise between the flash and SAR-based A/R converters by using the principle of subranging. The area complexity is medium for the iterative flash A/R converter. The conversion speed is $p + 1$ extended clock cycles where '$p$' is the number of iterations in which the first flash stage performs conversion. The two-stage flash-like subranging converter (Lojacono 2004) using the principle of calliper rule also requires high area but operates faster. The ΣΔ based A/R converters provide high speed conversion at oversampling rate. For every clock cycle, the modulator produces output which is filtered and downsampled by the decimation filter to produce residues at Nyquist rate. It has medium hardware complexity compared with other existing A/R converters. The proposed A/R converter based on a ΣΔ modulator provides high conversion speed, high resolution and a low cost implementation. The performance of the ΣΔ based A/R converter is compared with the Nyquist rate A/R converters in Table 3.

The approximate block level analysis shows that the ΣΔ based analogue-to-residue converter takes approximately 1.6 times the area of that for a successive approximation based converter. However, the increased area is justified because of the extra flexibility that the proposed converter gives. Further, due to the very basic nature of the ΣΔ converter, the anomalies in the anti-aliasing filter (the filter used before a signal sampler) of the A/R converter can be tolerated. In other words, a relaxed anti-aliasing filter will be sufficient for this new architecture.

## 4. Conclusion

A ΣΔ based parallel analogue-to-residue converter is proposed in this article. It exhibits superior performance over Nyquist rate A/R converters in terms of high resolution, high conversion speed and low cost implementation. The RNS-based decimation filter channels generate all residues in parallel and hence the whole conversion operation becomes faster. The proposed approach that trades quantiser resolution for oversampling using analogue integration and negative feedback could be a better choice for digital CMOS processes focusing on high speed devices at reduced supply voltages. The proposed A/R converters could find significant application in wideband wireless communication for high resolution and high speed data conversions.

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