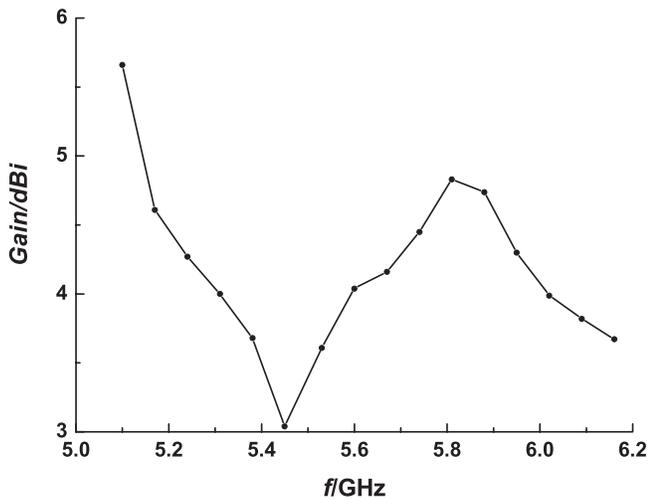


(a)



(b)

Figure 6 Peak gain of the proposed dual-band antenna (a) 2.4-GHz band and (b) 5-GHz band

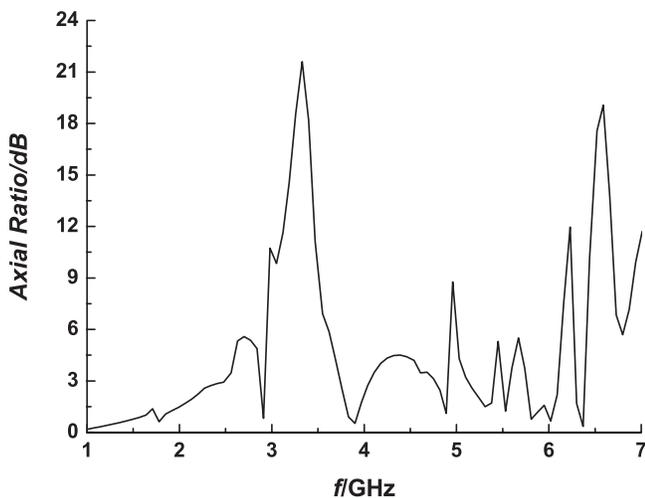


Figure 7 Axial ratio of the proposed dual-band antenna

integrated with other RF front-end circuits. Computer simulations and measurements have indicated that it can effectively cover WLAN operation bandwidth with circular polarization and the gain of the proposed antenna can meet the requirements of indoor wireless applications.

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ACS FED PRINTED F-SHAPED UNIPLANAR ANTENNA FOR DUAL BAND WLAN APPLICATIONS

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ABSTRACT: An asymmetric coplanar strip (ACS) fed dual band F-shaped antenna covering the 2.4/5.2 GHz WLAN bands is presented. The optimized dimensions of the proposed uniplanar antenna are 21 mm × 19 mm when printed on a substrate of dielectric constant 4.4 and height 1.6 mm. The dual band nature of the antenna is brought about by the various current paths in the F-shaped structure and the ground plane. The antenna exhibits nearly omnidirectional radiation characteristics and moderate gain in both the operating bands. Details of the antenna design, simulation, and experimental results are presented and discussed. © 2009 Wiley Periodicals, Inc. *Microwave Opt Technol Lett* 51: 1852–1856, 2009; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.24486

Key words: ACS feed; dual band; uniplanar antenna; WLAN antenna

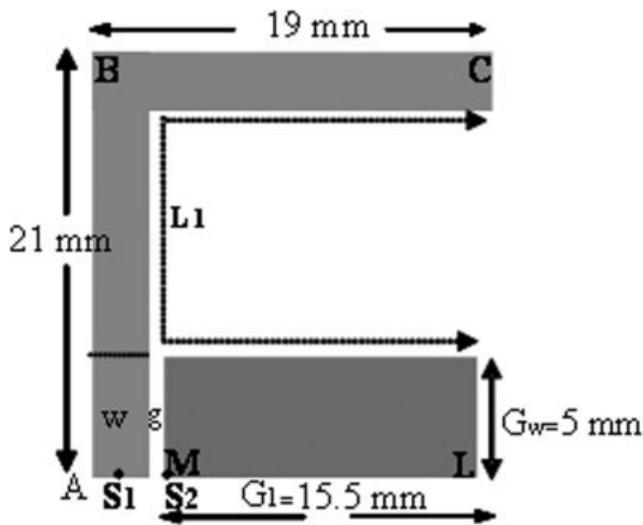


Figure 1 ACS fed inverted L antenna

1. INTRODUCTION

The rapid growth of wireless internet for high data rate communication has fostered tremendous attention toward the design of compact WLAN antennas. Different types of designs catering to various user requirements have been reported in literature [1–4]. These designs, however, have complex structures which make them difficult to integrate with WLAN systems. Uniplanar antennas have the advantage of easy integration with active circuits. Many types of uniplanar antennas have been reported in literature [5]. In this article, we present an Asymmetric Coplanar Strip (ACS) fed F-shaped dual band antenna. The uniplanar nature, simple feeding technique, and compact structure of the antenna presented in this article, make it easy for modular design. Ansoft HFSS V10 is used for the simulation and analysis of the structure. The resulting antenna operates from 2.24–2.55 GHz and 4.64–5.39 GHz covering the 2.4/5.2 GHz WLAN bands. In the first section, an inverted L-shaped antenna is discussed. An additional strip is added to the above structure to produce a dual band F-shaped antenna design.

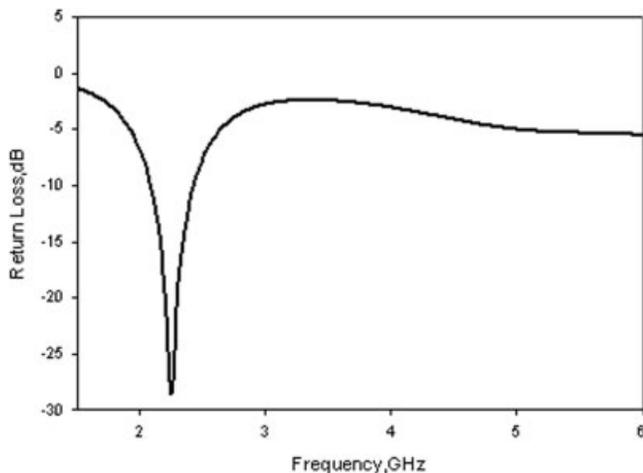


Figure 2 Return loss curve of the ACS fed inverted L antenna

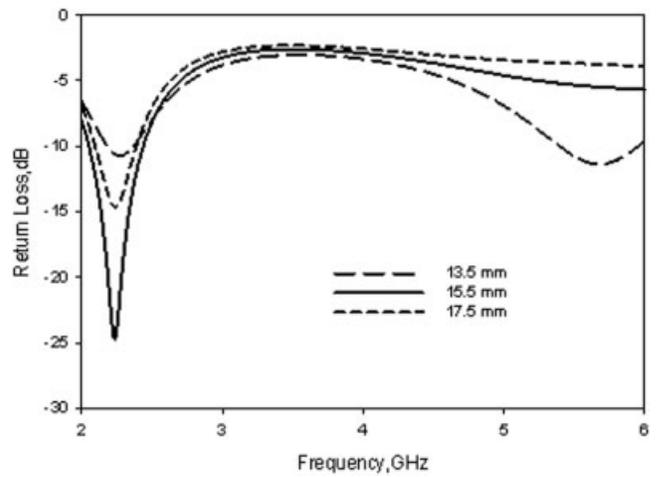


Figure 3 Effect of varying the Ground plane length (LM) of the ACS fed inverted L antenna

2. EVOLUTION OF THE ACS FED F-SHAPED MONOPOLE ANTENNA

2.1. The Inverted L Antenna

In this section, the evolution of the final F-shaped antenna from a simple inverted L antenna is discussed. An open circuited Asymmetric Coplanar Strip can be used as an effective feed for uniplanar antennas. To design a simple ACS fed antenna a meandered, simple inverted L structure is fed using the ACS as shown in Figure 1.

The inner feed conductor of the coaxial cable is connected to the point S1 and the outer ground is connected to S2. The width of the signal strip “ w ” = 3 mm and the gap “ g ” = 0.5 mm of the ACS transmission line are derived from standard design equations [6] and is found to be 62Ω . After exhaustive experimental studies, it is found that for better impedance matching of the whole system the ACS transmission line impedance has to be between 60 and 70 Ω . The return loss characteristics of the inverted L antenna are shown in Figure 2. The antenna resonates at 2.3 GHz with a 2:1 VSWR band width of 340 MHz. This occurs when the inner edge length marked as L_1 is equal to half wavelength in the substrate. This can be achieved for various combinations of AB, BC, and LM. However; these lengths are optimized keeping in mind the

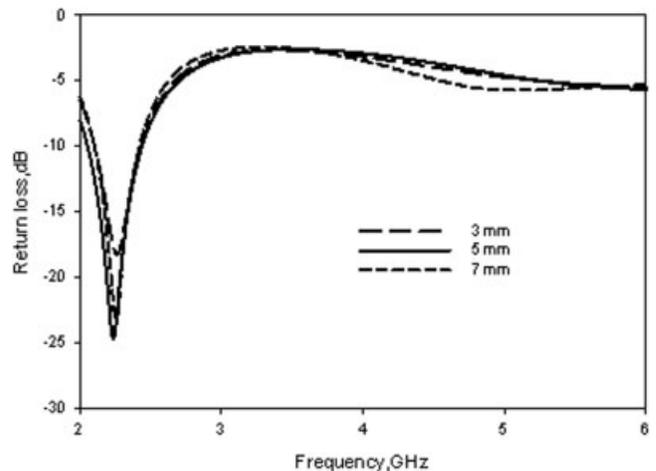


Figure 4 Effect of varying the Ground plane width KL of the ACS fed inverted L antenna

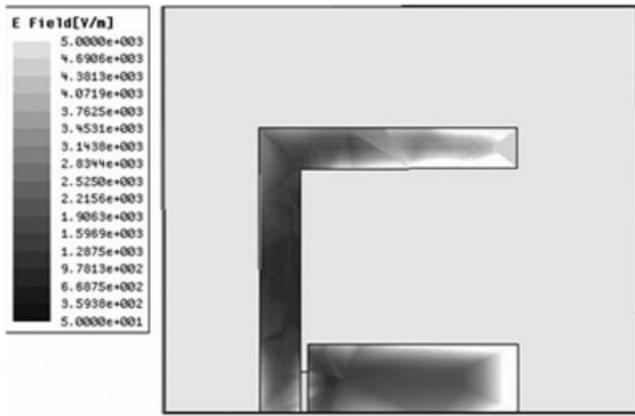


Figure 5 Field distribution in the ACS fed monopole antenna

compactness of the antenna. In our studies, the length AL , is taken to be equal to BC .

The ground plane optimization studies of the antenna keeping " L_1 " constant are as shown in Figures 3 and 4. It can be seen from Figure 3 that the length of the ground plane GL has profound influence upon the impedance matching of the antenna for constant L_1 . However, this much variation in return loss is not observed for ground plane width GW as demonstrated in Figure 4.

1.2. The Final Inverted F Antenna

The inverted L antenna discussed above exhibits only a single resonance centered at 2.3 GHz. To obtain an additional resonance in the structure without affecting the compactness of the antenna, another strip IH is attached to the above inverted L structure at minimum field intensity as shown in Figure 5 resulting in an F-shaped antenna (Fig. 6).

The second resonance at is due to the current path L_2 (Fig. 6). The length of IH is chosen so as to obtain the resonance at 5 GHz. The resulting return loss curve is shown in Figure 7. In this case, too L_1 corresponds to half of the dielectric wavelength at 2.34 GHz and the current length L_2 is equal to 0.60 times the dielectric wavelength at 5 GHz. The increase in the resonant path for the second resonance is due to the capacitive coupling between the strip IH and the ground plane. The variation of impedance of the antenna with offset position strip IH is shown in Figure 8. From

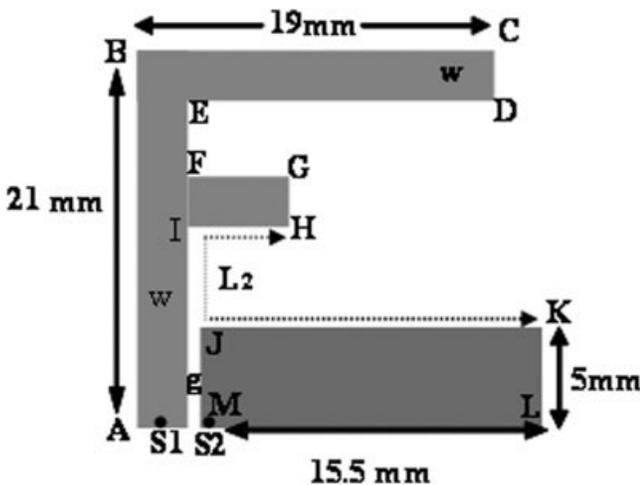


Figure 6 ACS fed inverted F antenna

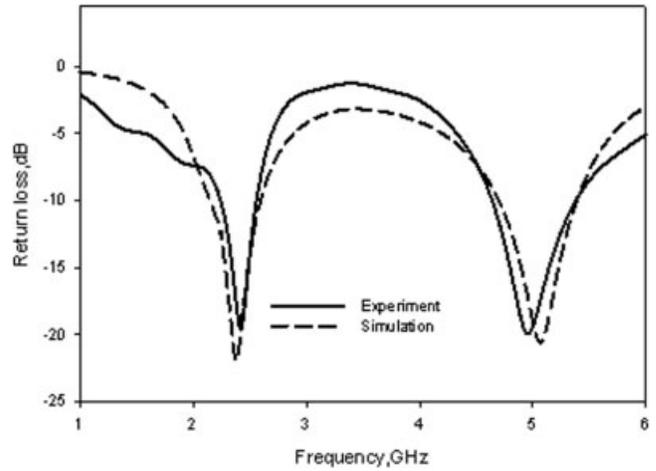


Figure 7 Experimental and Simulated return loss curve of the ACS fed inverted F antenna

our observation, it is concluded that the upper strip FED is acting as a stub at 5 GHz and improving the matching.

3. RESULTS AND DISCUSSION

The final ACS fed F antenna was constructed and tested using HP8510C vector network analyzer and the results are presented in this section. The experimentally observed 2:1 VSWR bandwidth of the antenna is from 2.24 to 2.55 GHz and from 4.64 to 5.39 GHz. The experimental results are found to be in agreement with the simulation results (Fig. 7.)

The radiation patterns of the antenna for the two bands in the principal planes are shown in Figure 9. The slight tilt in the XZ pattern at 2.34 GHz (due to L_1) is due to the asymmetrical nature of the dipole (L_1) with unequal arms, whereas at higher resonance the current path (L_2) is approaching the symmetrical nature and hence the pattern is like that of a symmetric dipole. Also, it is found that the antenna is polarized along the Y axis for the first

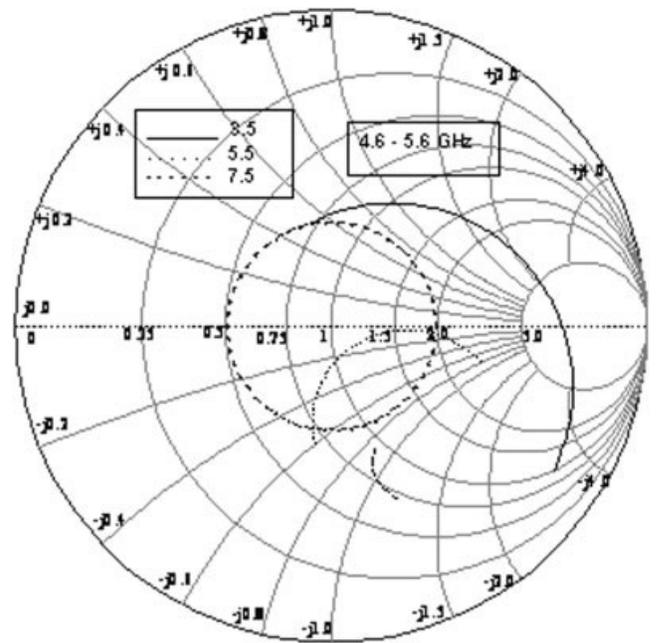


Figure 8 Effect of varying the height and position of the strip IJ

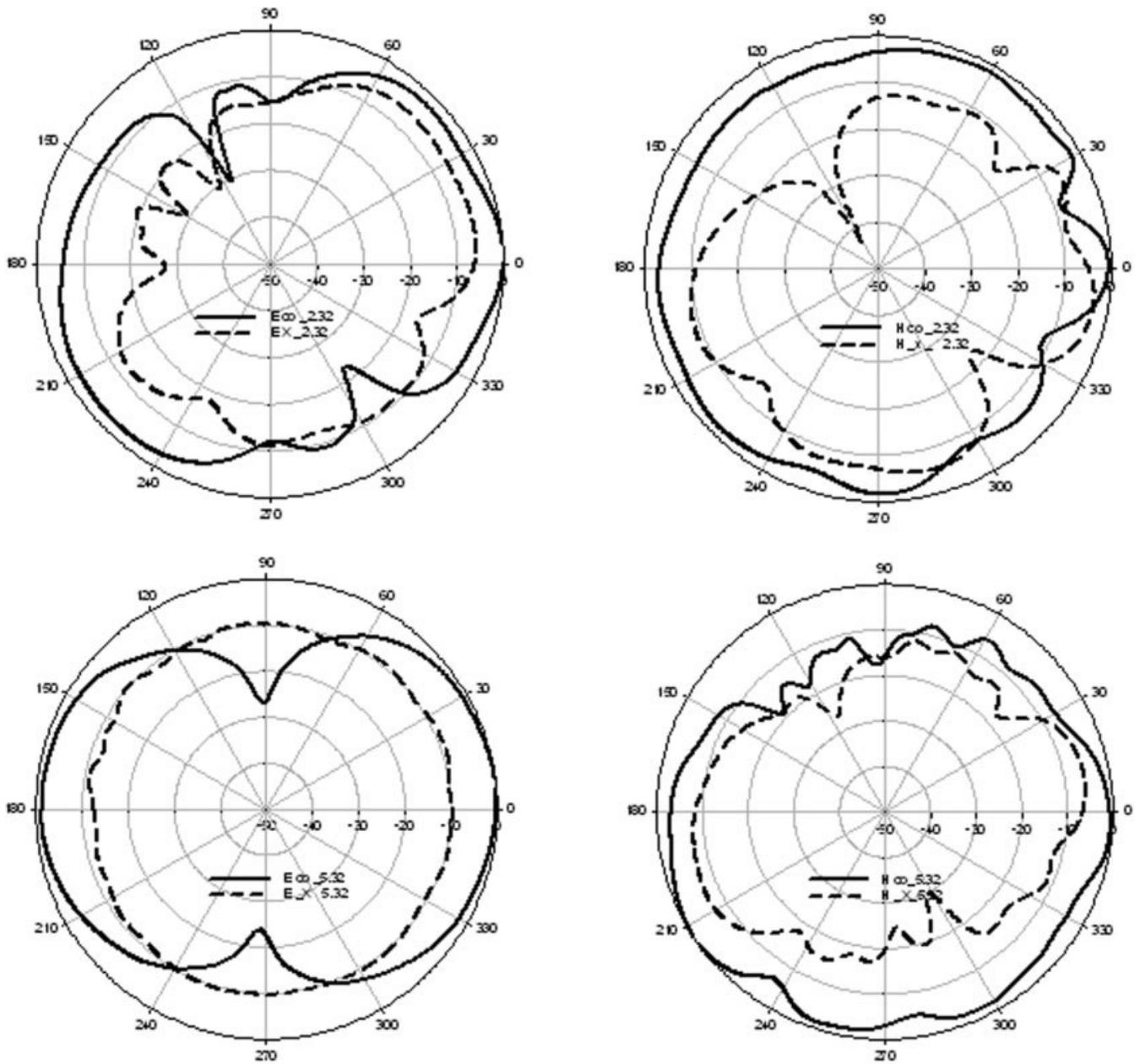


Figure 9 (a) XZ pattern at 2.4 GHz, (b) YZ plane pattern at 2.4 GHz, (c) XZ pattern at 5 GHz, and (d) YZ plane pattern at 5 GHz

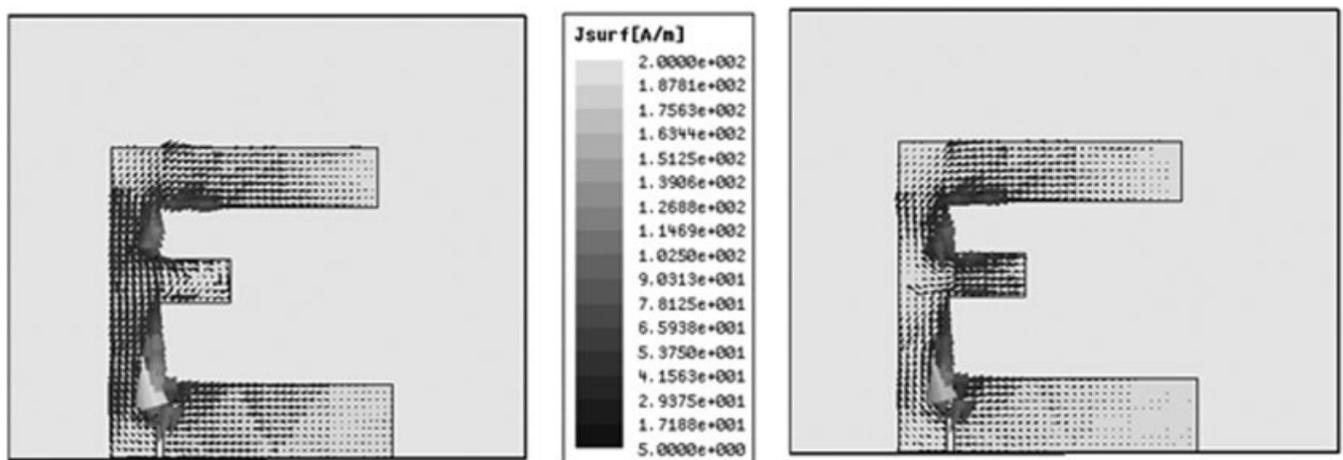


Figure 10 (a) Current distribution at 2.4 GHz and (b) Current distribution at 5 GHz

band and along the X axis for the second band. This is because at the first resonance, the current illumination is along AB [Y axis Fig. 10(a)]. At the second resonance, the Y directed currents along EF and IH are in opposite directions and cancel at far field [Fig. 10(b)]. Hence, the radiation is purely due to the X -directed dominant current along IH.

The measured gain of the antenna is equal to 1.9 and 1.7 dBi at 2.34 and 5 GHz, respectively with an average efficiency of 74%.

4. CONCLUSIONS

The article presents an asymmetric coplanar strip fed F-shaped monopole antenna for dual band applications. The antenna has a uniplanar structure and compact dimensions of 21 mm \times 19 mm \times 1.6 mm when fabricated on an FR4 substrate of dielectric constant 4.4. The parametric optimization of the antenna is performed. An omnidirectional radiation characteristic with moderate gain is also noted. The simple structure, compact dimensions, and integration to active and passive circuits make it an ideal candidate for wireless applications in the 2.4/5.2 GHz WLAN bands.

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LOW-LOSS AND HIGH-ISOLATION ACTIVE TYPE CASCODE SWITCH IN 0.13- μ m CMOS FOR MILLIMETER-WAVE APPLICATIONS

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ABSTRACT: This article presents two types of switches which are fabricated in 0.13- μ m standard CMOS process characterized up to 50 GHz. The first is the conventional series NMOS switch with an optimum gate width which is adjusted by measuring various sized devices. The second is a new active type cascode switch for millimeter-wave phased array systems. The series NMOS switch produces 3 dB insertion loss and 7.5 dB isolation at 40 GHz. In contrast, the active type cascode switch has 7.5 dB better insertion loss (Gain) and 20 dB better isolation

than the passive switch at 40 GHz. © 2009 Wiley Periodicals, Inc. *Microwave Opt Technol Lett* 51: 1856–1858, 2009; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.24476

Key words: active switch; CMOS switch; 0.13- μ m CMOS technology; millimeter wave

1. INTRODUCTION

Electronic switches, the important building blocks in millimeter-wave phased array systems, have been traditionally developed using III-V semiconductor-based transistors or diodes. Although III-V semiconductors give low insertion loss and high isolation, their cost and integration considerations motivate the development of CMOS solutions. Recently, CMOS technologies have been scaled down to become good candidates for low-loss designs below 5 GHz [1]. However, CMOS switches above 10 GHz still exhibit high insertion loss and low isolation [2–5]. Dual switch configuration with series-shunt connected FETs is common designs for obtaining improved isolation. However, the insertion loss of the dual switch cannot be lower than that of the single series switch [4]. Although there are some reports about the use of high substrate resistance networks to decrease the insertion loss [1–4], the result in [4] shows only 0.8 dB improvement at k-band. Additionally, a five-bit phase shifter using series NMOS switches exhibits 15 dB insertion loss at ku-band [5]. To implement a low-loss design above 40 GHz, we study a conventional series NMOS switch and a new active switch in 0.13- μ m standard CMOS process. It is found that the active switch could be a good candidate for millimeter-wave phased array systems, even though it requires DC power consumption and needs an extra matching network.

2. PASSIVE AND ACTIVE SWITCHES

Figure 1(a) shows a schematic of the conventional series NMOS switch. The Drain/Source is connected to the input/output port and the gate is biased through a 1 k ohm resistor to prevent RF signal leaking. The insertion loss and isolation is affected by the on-state channel resistance, the drain-source coupling capacitance, the source/drain junction capacitance and the conductive Si-substrate [3]. To improve insertion loss, the on-stage channel resistance is usually reduced by enlarging the gate width even though the isolation is sacrificed by a larger drain-source coupling capacitance. This means that there is an optimum gate width at the desired frequency range. We take 64- μ m (2 μ m \times 32 fingers) gate width for over 40 GHz phased array systems by simulating the various sized switches and measuring three different sizes (40, 64, 80 μ m) of switches.

An active switch, which uses the amplifier topology for an on/off switch, could be a good candidate to improve the loss of the passive switch. Cascode topology with common source and common gate [as shown in Fig. 1(b)] are quite popular for RF amplifiers. The cascode can be used as an active switch by controlling the voltage of the common gate by supplying the fixed DC voltages at the gate/drain of the common source/common gate. Before choosing the cascode topology, we investigated both the cascode and common source switches. The cascode produces 3 dB better maximum available gain (MAG) and 23 dB better isolation at Q-band than the common source switch with controlled gate voltage and fixed drain voltage.

Figure 2 depicts the layout of the cascode switch. We also take 64- μ m (2 μ m \times 32 fingers) gate width for both common source and common gate. The transistor layouts employ standard parameterized cell (p-cell) with deep N-well (DNW) from the foundry.