Design and Development of Interleaved Cuk Converter with Boost Facility for Multiple Output Voltages

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Doctor of Philosophy
under the Faculty of Engineering
By

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Ph.D Thesis under the Faculty of Engineering

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Certificate

Certified that the thesis titled **Design and Development of Interleaved Cuk Converter with Boost Facility for Multiple Output Voltages** submitted by Joseph K.D., is an authentic record of the research work carried out by him under my supervision for the award of degree of Doctor of Philosophy in Faculty of Engineering, Cochin University of Science and Technology. The work presented in this thesis or part thereof has not been presented for any other degree. All the relevant corrections and modifications suggested by the audience during the pre-synopsis seminar and recommended by the Doctoral Committee have been incorporated in the thesis

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Declaration

It is declared that the thesis titled **Design and Development of Interleaved Cuk Converter with Boost Facility for Multiple Output Voltages** is an authentic record of the research work done by me under the guidance of Dr. Asha Elizabeth Daniel, Professor and Head, Division of Electrical Engineering, School of Engineering, Cochin University of Science and Technology and Dr. A. Unnikrishnan, Outstanding Scientist (Rtd), Naval Physical & Oceanographic Laboratory, Cochin. This work or any part thereof has not been presented to any other institution for any other degree.

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Abstract

DC - DC converters are one of the major component in most of the power electronic equipments. These converters find applications in switched mode power supplies, battery operated electric vehicles, LED drivers for lighting, DC micro grids, battery chargers, DC welding solar power conditioners, and power conversion equipments in DC transmissions, covering different ranges of power such as low, medium and high specifically for power conversion processes. The basic circuit topology for DC - DC converters offers the buck and boost facility, utilized for power handling. They provide pulsed currents either on input or on output side, due to the availability of inductor either at input or at output. The pulsed power affects the power quality, which is required is to be very high, to avoid injection of harmonics to the parent source. The problem is more precarious, when the DC - DC converters are used in large numbers in order to transfer the requisite amount of power. Naturally, the research investigations are focused in the key area like

1. reduction of ripple content,
2. peak current of switch,
3. current programmed/ voltage mode control,
4. design of compensator/ controller in closed loop,
5. design of the pulse width modulator,
6. modification converter circuit topology to obtain high gain and
7. optimization of efficiency.

The issues like communication and system level integration, zero power switching, restriction of number of components and their sizes and over all thermal management have also received wise attention among the research community.

The requirements as required above are yet to be realized fully the designs of the DC - DC converters currently available. While the wish list of any industry demanding a promising performance on the DC - DC converter, includes ripple free current at output, along with tight regulation and high efficiency. Accordingly the author is motivated to investigate the design and development of new topology for the DC - DC converter to offer simultaneous boost and buck operation, also providing stable operation and effective switching to reduce the ripple, confirming high power quality.

In this context, while exploring the available topologies for the DC - DC converter, it is seen that the Conventional Cuk Converter (CCC) has received wide appreciation in the present day DC - DC converter designs, both in research and industry. The Cuk converters are noted for the configuration, offering better characteristics on ripple content of currents, compared to all basic DC - DC converters, due to the presence of inductors on both input and output sides. Obviously the resulting continuous current is taken as the candidate for performance analysis and so the components of CCC are designed by considering ripple current and ripple voltage. In order to provide stable output with a tight regulation, a compensator is also included in the feed back path to operate the complete system in closed loop. On simulation and hardware validation of CCC in closed loop in continuous conduction mode, it is observed that this converter produces large current ripple on input side, which affects the quality of source and in turn reduces the life of connected equipments/devices. While the operation is better in the buck mode with duty ratio less than 0.5, this converter can provide step-up of

input voltage only when the duty ratio is beyond 0.5. Also when CCC operates with duty ratio above 50%, the switching current is high, so as to heat up the switching devices. The efficiency and the regulation were also not quite acceptable in the basic CCC. Accordingly, an Interleaved Cuk Converter (ICC) with Phase Shifted Pulse Width Modulation (PSPWM) is proposed in the thesis. The proposed configuration is designed in the buck mode to reduce the input current ripple and also to improve transient performances. The design of the Proposed ICC is complete with a digital type III compensator fused in a FPGA controller in the feedback path, in continuous conduction mode. The design is also simulated and realized in hardware. The interleaved feature shares the current and offers inbuilt ripple cancellation, which improves the quality of source current. The decrease in ripple content also reduces associated losses and improves the converter efficiency. A PSPWM technique is developed to decrease duty ratio to half, which has helped to reduce the switching current during transitions. Also the proposed converter provides improvement in transient performance with overshoot and settling time. The switching stress is appreciably less for the Proposed ICC, when it is operated for buck mode of operation, with effective ripple cancellation.

But boost mode of operation creates overlap of PSPWM switching pulses, which builds ripples on source currents due to simultaneous charging or discharging of inductors. Hence the operation of the Proposed ICC is limited for buck operation only, to provide two parallel outputs with ripple cancellation.

With a view to achieve boost operation also with low switching stress and high efficiency, the thesis has come up with a modification on the Proposed ICC topology, to provide step-up of input voltage with duty ratio less than 0.5, by judiciously employing the PSPWM scheme. So the Modified Interleaved Cuk Converter (Modified ICC)

is demonstrated to achieve both boost and buck operations, with multiple power outputs, with ripple content much lower than the CCC and the Proposed ICC. Here again the Modified ICC is designed with digital compensator in the feed back path. The circuit is simulated and experimentally validated by realizing the hardware. The digital compensator has been realized in a FPGA SPARTAN 3AN Altium Nano board. The experimental validation in hardware in closed loop, by voltage mode control of the converter, shows that the converter has multiple different variable outputs and the third output is obtained by summing two interleaved output voltages. A note worthy feature of this parallel input series output converter is that the overall switching current stress, input current ripple and losses are reduced, appreciably well below the CCC and the Proposed ICC. The efficiency and the transient performances are also improved along with better output voltage regulation.

The thesis has therefore reported the design of an improved version of a DC to DC converter, offering multiple outputs so as to take care of both buck and boost operations. The reduced ripple content, high efficiency, tight regulation and low switching stress are the added traits of the new design reported. The circuit is also realized in hardware and performance is evaluated with two other configurations, popular in literature. The contents of the thesis have been communicated to standard literature and some of the papers communicated have already been accepted for publication after extensive review.

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List of Abbreviations

ADC	Analog to Digital Converter
CCC	Conventional Cuk Converter
CCM	Continuous Conduction Mode
CLC	Capacitor Inductor Capacitor
DCM	Discontinuous Conduction Mode
DPWM	Digital Pulse Width Modulation
d-q axis	direct -quadrature axis
DSO	Digital Storage Oscilloscope
FPGA	Field Programmable Gate Array
HVDC	High Voltage Direct Current
IC	Integrated Circuit
ICC	Interleaved Cuk Converter
LCL	Inductor Capacitor Inductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PI	Proportional Integral
PID	Proportional Integral Controller
PWM	Pulse Width Modulation

PSPWM	Phase Shifted Pulse Width Modulation
RB	Reverse Bias
SEPIC	Single Ended Primary Inductor Converter
THD	Total Harmonic Distortion
VSC	Voltage Source Converter
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

List of Symbols

d	Duty ratio
d_1	Duty ratio of first switch S_1
d_2	Duty ratio of second switch S_2
I_g	Source current
I_{1a}	Current through the inductor L_{1a}
I_{2a}	Current through the inductor L_{2a}
I_{1b}	Current through the inductor L_{1b}
Ii_{2b}	Current through the inductor L_{2b}
I_o	Output current through the load resistor R_L
V_{L1a}	Voltage across the inductor L_{1a}
V_{L1b}	Voltage across the inductor L_{1b}
V_{L2a}	Voltage across the inductor L_{2a}
V_{L2b}	Voltage across the inductor L_{1b}
V_g	Source voltage
V_{c1}	Voltage across the capacitor C_1
V_{c2}	Voltage across the capacitor C_2
V_{o1}	Voltage across the capacitor C_{o1}
V_{o2}	Voltage across the capacitor C_{o2}

V_o	Voltage across the load resistor R_L
ΔI_g	Ripple on source current
ΔI_{1a}	Ripple current through the inductor L_{1a}
ΔI_{2a}	Ripple current through the inductor L_{2a}
ΔI_{1b}	Ripple current through the inductor L_{1b}
ΔI_{2b}	Ripple current through the inductor L_{2b}
ΔI_o	Ripple on output current through the load resistor R_L
ΔV_o	Ripple on output voltage
t_{ON}	ON time of switch
t_{OFF}	OFF time of switch
T_s	Switching time period
μ	micro

Chapter 1

Introduction

1.1 Motivation

Though the bulk power generation in the world so far have been largely on the AC side, many utilities have been developed on DC power source. Ever since the digital systems comprising of computers, controllers and the signal processing and communication processing platforms chose to remain digital, there has been an increasing demand in the industry for DC sources, with different output voltages. With the advent of semiconductors being available for high voltage and high current switching applications, the industrial drives also started looking for DC power sources. With the dawn of digital transmission of high voltages, the need for DC to DC converters became a well sought out technology, by Power System Engineers also. The modern world is blessed to be in an era, where enough DC sources are directly available from Solar PV systems, fuel cells and high density batteries, making it possible to derive DC

voltages directly a DC source. As one looks back into the history, the earlier approach to convert the voltage of a DC supply to a higher voltage, specially for low-power applications, was to convert it to AC by using a mechanical vibrator, stepped up by transformer and rectify to the required specifications [1], [2]. For producing higher power, an electric motor was used to drive a DC generator for the desired voltage. Obviously all these methods proved out to be inefficient, bulky and expensive, which often became an unavoidable imposition. The developments in power semiconductors and integrated circuits, made it possible to directly convert DC input to DC output. The boost and buck operations as they called popularly named in the DC-DC converter parlance, resulted in economically viable solutions for converting DC voltages.

The DC - DC converter is one of the most sought out devices in the present era, thanks to the ready availability of DC power from multitude of energy sources including the non-conventional ones. The DC DC converter primarily converts voltage on one level into another level by switching the incoming supply line. Inductors and capacitors are also part of the circuit to ensure energy transfer and delivery of steady voltage at the output, with minimum disturbance at the input as well. Conventional DC - DC converters are having only one inductor on DC side and which reduces ripple at the output to a certain extent. However sharing the current by connecting inductors in parallel often reduces the size and value of inductors, in those cases where the requirement to carry the required higher source currents demands larger rating of switches and size of the inductor. The paralleling becomes a blessing which reduces the ripple content on current by cancellation technique. While the switches in converters are turned ON and OFF by high frequency switching to improve the shape of average output voltage, a properly designed Pulse Width Modulation (PWM) can ensure effective ripple

cancellation, thereby improving the output voltage profile as well. However, one must be cautioned against the possibility of ripple building issues, which may turn out be counter productive, because of improper selection of the frequency and the design of the of PWM logic. The current sharing not only improves the current shape but also reduces the magnitude of current to be carried by each component in input side. The reduction of size of the components reduces the weight of the converter hence the DC - DC converter can be used with high current utilities.

The high frequency switching of high currents, which is inescapable in DC to DC conversions, can tell upon the power quality. Power quality is a matter of primary concern, when power electronic equipments are used specially in power systems. The contentious issue here points to the non-linearities of switching in power electronic circuits, which can cause harmonics in source current, directly hampering the power quality. The non-linearities stem out of the non linear characteristics of semiconductor switches and gets worse when used with storage devices like inductors and capacitors, which also have limitations in providing linear characteristics all the time. It is well acknowledged fact that the output voltage/current signals of the power electronic circuit not often in the required sinusoidal shape and therefore can not be directly applied to all types of utilities. In order to overcome the problem, electric filtering circuits are designed and inserted before the utility equipment. These power electronic equipments/ components can also produce distortion on input side source current waveforms apart from the output voltage. Generally series input inductors are used to filter the input current, while parallel output capacitor filter frequently improves the output voltage profile. Commonly harmonic filters are designed to ward off high frequencies on ac side. As in the well known case of the traditional rectifier circuit, a large capacitor filter

improves the shape of output voltage profile; but including the harmonic filter on the input side improves the source current shape and the input power quality. The filters designed for high frequency have the added advantage of lower size. Also the converter with filters on both sides can be generally used in power system to improve the power quality. The ripple produced because of the switching in power electronic circuits thus gains prominence while discussing the design of power electronic circuits, especially of applications demanding large currents.

In the attempt to reduce the ripple content resulting from the switching circuits, a good number of circuits have appeared in literature. They include paralleling and interleaving to provide the ripple cancellation. Many of these circuit topologies have evolved as part of the development in the DC - DC converters. The ever increasing demand to provide ripple free power, with multiple output voltages from a single source at the same time limiting the size has been a major challenge to the designer of power systems. It is in this context that the present study is taken up to provide effective solutions to all the issues raised above.

1.2 Introduction

Taking a look at the DC - DC converter circuit technology, a DC - DC converter transforms a DC voltage in to another DC voltage, with lower or higher magnitude. The demand for DC - DC converters are on the increase in industry, electric drives, traction and in power transmission. DC - DC converters have already found a stable place in switched mode power supplies in laptop and desk top computers, digital television set and a host of practical utilities like

surveillance systems, medical gadgets, battery chargers in electric vehicles and locomotives. Sensing the ease of using DC power, the conversion equipments in power transmission and micro grids are also suing the DC to DC converters in various voltage levels and power capacity.

The basic topologies of DC to DC converters utilize the high current switching technology using semiconductor switches, thereby generating pulsed currents either on input or on output or even both. The high frequency used in switching high currents can pose a serious challenge to the quality of power both at the source and the utility. Apart from creating pulsed and distorted signal waveforms at the utility end, the non-linear operation of switches also creates ripples in both at the input and output of the DC to DC converter. With large number of DC to DC converters operating in a system, the input ripple can also lead to serious harmonic distortion of the parent source. The present day industry demands high efficient power converters with low ripple and better transient performance, with an uncompromising rider on the power quality.

1.3 DC - DC Converter Circuits

The basic DC-DC circuits are buck, boost and buck-boost converters and a review [3] of these converter circuits would be in order to appreciate the rest of the thesis. A typical buck converter is shown in Fig. 1.1, which steps down a DC voltage. The converter circuits have semiconductor switch, storage devices like indictors and capacitors and the pulsing circuits to regulate the switching process.

As shown in Fig. 1.1, Inductor L is charged from the source DC voltage V_g when the switch S is turned ON and transfers stored energy to load

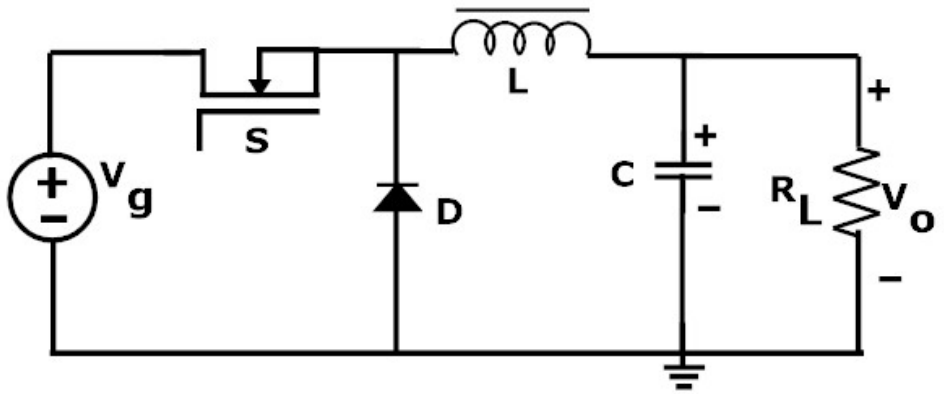


Fig. 1.1: Circuit diagram of ideal buck converter

resistor R_L through the diode D and filter capacitor C, when the switch S is turned OFF. So the output voltage has the step down operation [4] as described by the Eqn.(1.1).

$$V_o = d * V_g \tag{1.1}$$

where d, $0 < d \leq 1$, is duty ratio. The inductor L in the buck converter filters the output current to smoothen it. But the absence of an inductor on input side results in pulsed input current.

A boost DC-DC topology is shown in Fig.1.2, which steps up a DC voltage. The inductor L is charged from the source DC voltage V_g when the switch S is turned ON. Due to the negative polarity of L the diode is reverse biased at this time. But when the switch is turned OFF the diode becomes forward biased and transfers the sum of stored voltage in L and input voltage to load resistor R_L. The capacitor C filters the output voltage to reduce ripple content. So the output voltage is the stepped up [4] by Eqn. (1.2).

$$V_o = \frac{V_g}{1-d} \tag{1.2}$$

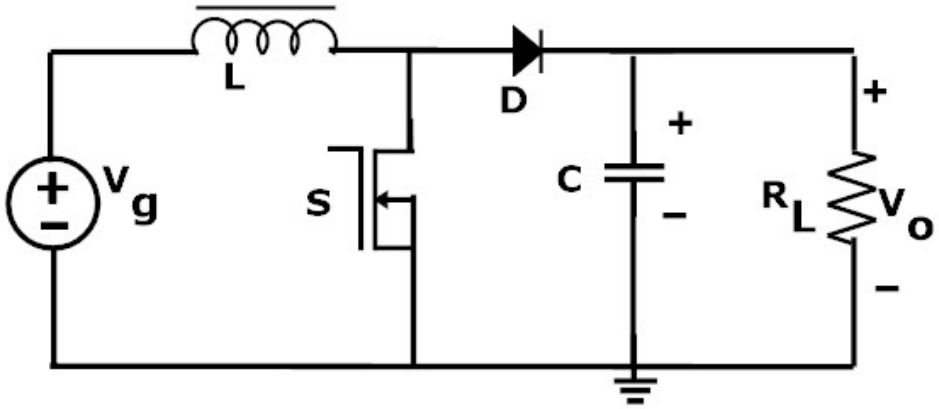


Fig. 1.2: Circuit diagram of ideal boost converter

where d, 0 <d $\leq$ 1, is duty ratio. The inductor L in the boost converter filters the input current but the absence of inductor on output side causes pulsed output current.

The combined buck-boost DC-DC converter circuit is shown in Fig.1.3, which can perform step up/down a DC voltage source. The output voltage has opposite polarity with respect to the input voltage. The Inductor L is charged from the source DC voltage V_g when the switch S is turned ON. Due to the positive polarity to the cathode, the diode D is reverse biased at this time. When the switch is turned OFF the diode becomes forward biased by the inductor and transfers stored energy to load resistor R. The capacitor C filters the output voltage to reduce ripple content. So the output voltage [4] is given by Eqn. (1.3).

$$V_o = \frac{d * V_g}{1 - d} \tag{1.3}$$

where d, 0 <d $\leq$ 1, is duty ratio. It can be seen that the boost or buck operation is possible with the value of d, properly chosen. d < 0.5

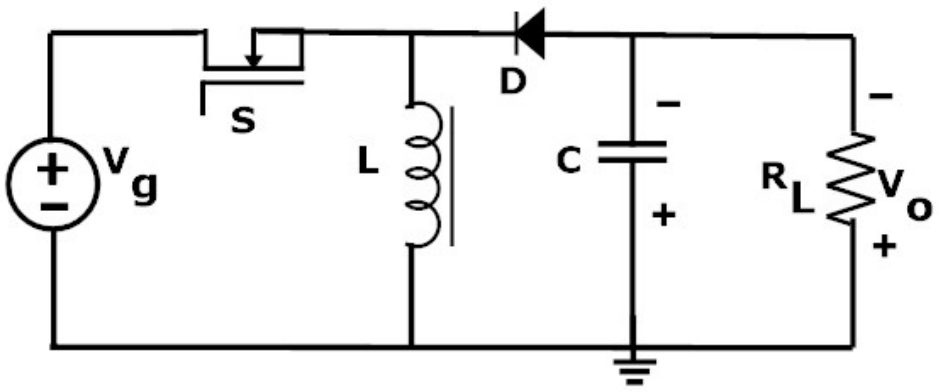


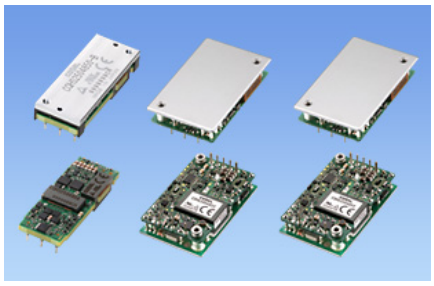
Fig. 1.3: Circuit diagram of ideal buck boost converter

bucks the output voltage while d > 0.5 results in boost operation. Here again the absence of inductor at the input is not quite an acceptable feature.

Industrial DC - DC Converters are manufactured and supplied by M/S Cosel, Japan [5] for medical applications viz. ventilator, incubator, artificial heart pumping in hospitals. A 120W single input multiple output DC - DC converter is shown in Fig. 1.4a and various industrial DC -DC converters are shown in Fig. 1.4b. The multiple output converters are used for a single medical equipment with its different variable utilities. The converter in Fig. 1.4b operates with an input voltage range of 36V - 76V with an output of 50V. It is operating with a current range of 5A to 7.9A with in the power range of 250W to 350W.

One of the basic restrictions of the converter topologies reviewed so far is the difficulty to get continuous currents both at the input and output. The limitation leads to the generation of ripples in the converter circuits, that can seriously hamper the power quality. In

(a) Single input multiple output DC - DC converter



(b) Various DC - DC converter packages

Fig. 1.4: Industrial DC - DC Converters; *Courtsey : Cosel Co. Ltd, Japan*

this context, the Cuk converter with continuous input and output current has been a very popular topology in literature [6], [7], [8] and is therefore taken as the potential candidate for investigations in this thesis.

The Cuk converter is one of the buckboost type DC -DC converter which produces the output voltage with opposite polarity to input. An ideal Cuk converter is shown in Fig. 1.5, which operates based on energy transfer by capacitor. The inductor L_a is charged when

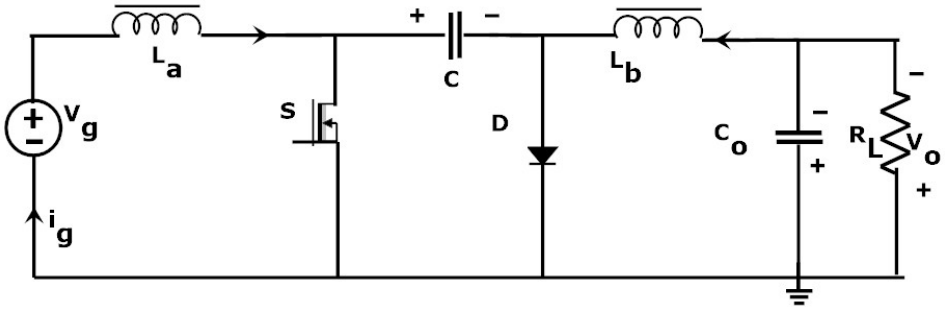


Fig. 1.5: Circuit diagram of ideal Cuk converter

the switch S in ON state and the capacitor C is discharged. And at the same time the output capacitor is also discharged and the filter inductor L_b is charged. When the switch is in OFF state the inductor L_a discharges and the capacitor C is charged. Also the capacitor C_o is charged and the inductor L_b is discharged. During the OFF state the capacitor stores energy and trnsfers to the output during the ON state. The output voltage [4] is given by Eqn. 1.4.

$$V_o = \frac{d * V_g}{1 - d} \tag{1.4}$$

The Cuk converter design is noted for better characteristics on ripple content of currents, compared to all basic DC - DC converters. Low source current ripple has been an enabling factor in the choice of the Cuk converter adequate requirement when these converters are deployed in large numbers in various applications. Even though the current is continuous in Cuk converter, the presence of noticeable amounts of ripples on input current is an accepted fact in the design. The large ripple currents on source side in Cuk design require large filter on input side to reduce harmonics, to improve distortion factor and thus to enhance power factor and efficiency. Also the power rating of the switching devices and passive elements have to be reduced for conversions in high power transmission lines and in high current applications. It thus turned out that the DC to DC Converter design needs further investigation, to provide attractive features like found that ripple current cancellation, zero power switching, low-switching stress, high gain converter with high efficiency and low ripple on voltage and current both at input and output.

One of the effective approaches reported [9] in the DC - DC converter designs to improve the power quality is the interleaving of the converter circuits. The interleaving strategy decides the amount

of the current can be shared, which helps to reduce ripple on source current, simultaneously bringing down the size and rating of the devices. Accordingly the investigations in the design of isolated DC - DC converter during last two decades are largely focused in evolving the circuit topology to enhance the quality of input and output currents, besides tangible improvement in voltage characteristics and efficiency, with better transient and dynamic performance.

The current sharing and ripple cancellation features are part of Cuk converter design, called the Interleaved Cuk Converter. In order to alleviate the above mentioned issues an Interleaved Cuk Converter (ICC) using Phase Shifted Pulse Width Modulation (PSPWM) scheme is proposed. The Proposed ICC operates comfortably below duty ratio 0.5 and it cancels the ripple content on source current effectively. Interleaved converters can also operate beyond a duty ratio of 0.5 for boost applications; but the ripple building issues created are not a very attractive feature. Hence Proposed ICC are known to provide buck operations only, since the switch can be effectively operated up to a duty ratio of 0.5. The simulation and experimental validation of Proposed ICC through hardware realization has demonstrated the improvement of current ripple on input side, reduction of ripples on both voltage and current on output side, reduction of current stress of switches and excellent transient performances, complete with better efficiency.

The drawback of the circuit of Proposed ICC in providing efficient boost operation is overcome in the thesis, by altering the circuit in to a novel topology called Modified Interleaved Cuk Converter (Modified ICC). Modified ICC is shown to provides both buck and boost output voltages with reduced source side current ripple. The converter provides three different output voltages, two are interleaved boost outputs and third is a buck output.

As part of the investigation, the power quality of the AC waveform is also assessed by driving the DC to DC converter developed, from an AC power source. For this, the converter circuits are extended to input side, by connecting through an uncontrolled bridge rectifier. The THD of the source current is evaluated and the power factor is measured to assess the input power quality.

1.4 Problem Definition

The discussions so far have brought out some of the major issues that need to be addressed in the development of the DC to DC converter. It is strongly felt that the design of the converter should

- guarantee high power quality, especially when basic DC to DC converters are used for power conversions.
- extend the capability of the ICC to provide boost operation, with reduced switching stress and high efficiency.
- improve the transient performance of the ICC. At present, the ICC gives better performance only during buck operations ($d < 0.5$), ICC has large peak switch current during boost operation and create ripple building issues with parallel outputs.
- come up with a modification on Proposed ICC, to provide boost operation not possible with ICC and
- provide multiple voltage outputs with tight regulation and high efficiency.

1.5 Objective

The observations made in the previous sections and the problem definition in Sec. 1.4, has motivated the author to take up the development of a DC - DC converter that promises reduced ripple and reduced switch current, along with high gain and high efficiency. The conflicting requirements as noted above, but supported by rich availability of literature on the Cuk converter, which brings out the good qualities of the Cuk Converter, were the inspiring factors that led to the development of the Modified ICC, elaborated in the thesis. Towards this, the rest of the thesis is organized as described below.

1.6 Organization of Thesis

Outlining the purpose, scope and the motivation of the thesis, **Chapter 1** is presented as an Introduction about power quality in general and DC - DC converters in particular. **Chapter 2** presents a comprehensive review of the relevant literature. This chapter covers brief description of the quality requirements of source current and output voltage, along with literature pertinent to related topics like the influence of PWM in the design of DC-DC converters and a general overview of the advantages and disadvantages of isolated and non isolated converters. Literature survey also brings out the gaps in the research area of converters vis - a - vis power quality

Since thesis has derived inspiration from the Cuk Converter, a detailed review of the traditional topology of the Cuk Converter is taken up in **Chapter 3**. Named as Conventional Cuk Converter (CCC), in the proposed thesis, the Chapter 3 focuses on the basic concept, followed by the detailed discussion of the operation of converter and the analysis

of the circuit, with comprehensive simulation. The stability of the closed loop converter is ensured with a suitable compensator for closed loop in voltage mode control.

In order to fully assimilate the behavior of the CCC, the hardware implementation of CCC is covered in **Chapter 4**. All the passive and switching components for the realization are carefully chosen or diligently designed. The complete operation of the circuit along with the XILINX Spartan 3AN FPGA Altium nano board implementing the compensator and wave form generator for PWM are demonstrated with Oscillograms displaying the various outputs. The valuable lessons form the implementation learnt from the hardware realization could reveal the limitation and gaps in the design of the CCC.

Chapter 5 concentrates on analysis of the Proposed interleaved Cuk converter (Proposed ICC) in closed loop in continuous conduction mode. The outcome of interleaving the Cuk Converter using PSPWM logic for switching is shown to bring in admirable reduction in ripple and switching stress especially in the bulk mode of operation. The results from the highly structured simulation of the circuit of the Proposed ICC underscored the above observation.

The findings in Chapter 5 were corroborated through the extensive hardware realization of the Proposed ICC in **Chapter 6**. The measurements as shown in the Oscillograms divulged the advantages of the Proposed ICC over CCC. The limitation of the Proposed ICC, in not being able to be operated in boost mode, could be brought out in this effort.

The major contribution of the thesis is discussed in **Chapter 7**. The chapter portrays the Modification of Proposed ICC, diligently done to improve the performance. The detailed analysis, design and simulation of the Modified ICC are discussed in this chapter. The complete design of the circuit with a type III compensator in the feed back path has

ensured the stable operation of the Modified ICC, with tight voltage regulation. The simulation results confirm the reduction in ripple, tight regulation, high efficiency and admirable transient response in the Modified ICC circuit developed in the thesis.

The hardware implementation of Modified ICC detailed in **Chapter 8**, has helped to reaffirm the findings of Chapter 7. The chapter ends with summarizing the merits of Modified ICC over other known converter topologies discussed in the thesis.

Chapter 9 consolidates the major findings of the thesis, vividly bringing out the contributions of the thesis. The major conclusions and directions for further research work are also provided in this chapter.

A major facet of the thesis is the hardware demonstration of all the circuits discussed in the thesis, thereby adding credence to the findings. The major results reported in the thesis have been published or communicated for publications in reputed journals and conferences, as shown toward the end of thesis.

Chapter 2

Review of DC - DC Converters

2.1 Introduction

The reduction of ripple content is an adequate requirement when DC - DC converters are largely employed for various applications like switched mode power supplies, electric vehicles, medical equipments, renewable and non-conventional energy conversions etc. The basic topologies buck, boost and buckboost converters have the inherent demerit of high ripple either on input or on output sides. The Cuk design reduces the ripple content due to the presence of energy storage and filter components on both input and output sides. The power rating of the switching devices and energy storage components have to be reduced when these converters are utilized in high power transmission lines and in high current applications. Moreover when the converters are operated above 0.5 duty ratio, due to the current stress impressed upon the switches, the rating, size and weight of converter are increased.

In such cases conventional DC - DC converter with lowest ripple on source side is not even useful since it will have high switching stress and higher current rating. Now the solution can be proposed as interleaved converter with low switch current stress and low current ripple compared to conventional converter. This thesis focuses on interleaved cuk converter which reduces ripple on source current due to its current sharing feature and also reduces peak current of switch of the power electronic devices. The reduction in ripple decreases harmonics on AC side and reduces Total Harmonic Distortion (THD) of source current, thus improves power factor.

2.2 Shaping of Source Current in Boost Converters

Sharing of current in two coupled inductors and two switching devices in the interleaved boost converter reported in [9], reduces the ripple content on input current by ripple cancellation technique. The two inductors and capacitors which are additional with conventional interleaved boost converter make the converter bulky. But the coupling of inductors in the converter gives a small reduction in the size and weight. The shared current reduces the magnitude of rated current through the components and switching devices. This reduces switch current stress and improves the dynamic performance. The ripple reduction reduces the losses thus the efficiency is also improved. Interleaved boost circuit with additional variable inductor [10] is utilized to regulate the output voltage with high gain. A double E-core is used to wind the variable inductor which causes to bulky converter and increased size. Also the losses associated with more number of components reduces the efficiency.

A simple boost non-isolated converter with coupled inductor topology [11] reduces the size and weight of the converter. The work reported in [12] for zero voltage transition of the switch is achieved by auxiliary capacitor circuit in coupled inductor boost converter. In the paper the conventional topology is modified by the additional coupled inductor and capacitor circuit to achieve high conversion ratio suitable for photo voltaic system. Interleaved boost DC - DC circuit with high voltage gain converter [13] reduces the ripple of source current at preselected duty ratio. The isolated input side inductors cancel the ripple and diode-capacitor arrangement improves the voltage gain. A third small inductor is used to control the current through diode. Although the number of components are limited to minimum which compacts the size of the converter, the increased number of components challenge the stability during transient conditions.

Parallel input series output interleaved boost converter presented in the paper [14] improves the output voltage by high gain. The switched capacitors on the output side, connected in series adds up the voltage. The switches are operated at zero voltage switching (ZVS) and diodes are operated by zero current switching (ZCS) to achieve zero power transition increase the efficiency. More number switches in the converter circuits compared with conventional interleaved boost converter adds to the complexity in circuit design and also in the PWM logic, making the converter bulky. The interleaved boost DC-DC converter with coupled inductor and clamping circuit [15] reuses the leakage energy of inductor. It reduces the switch voltage stress and also improves the efficiency of the converter. The circuit arrangement of inductors connected in series and the capacitor improves the voltage gain to a large extent without specially prepared PWM logic scheme. This circuit also regulates output voltage tightly with high gain and reduced ripple. Fast transient response of the circuit is an added trait in thid circuit.

Along with ripple reduction, the output voltage gain is improved with high efficiency in experimental result of interleaved high gain converter [16].

An interleaved bidirectional circuit with isolation transformer [17] performs zero voltage operation of switches throughout all loads improves the dynamic characteristics of the converter. The gain of the converter is designed to have high step-up/ down ratio according to the number of turns in coupled inductors. The additional coupled inductor in the circuit act as parallel for boost operation and series for buck operation which saves the transformer magnetic size. A derived logic of PWM with phase shift is used for triggering switches. The voltage stress of the switches are reduced by employing three level topology during high gain operation. The high step-up gain is achieved in the interleaved multilevel boost converter [18] with bidirectional flow of current. The multi parallel input reduces the ripple content in source current considerably. The switched capacitors on output with parallel-series combination increases the gain to many times the input voltage. The voltage stress of the switches is reduced to one-third in three level converter topology while the current stress on forward mode is eliminated by zero current switching. In the reverse mode the transition of the switches is not addressed and it draws a positive current. Also the number of switches in the one level circuit itself very high which leads to poor transient and dynamic behavior along with the demerit of high cost.

A novel circuit with auxiliary switch arrangement is used in compact interleaved DC-DC circuit [19] to achieve zero voltage transition on two switches. The series inductor circuit with diode and existing single capacitor combination meets the necessity of zero voltage at the time of switching for main two devices. Also the inductor provides zero current to auxiliary switch during the transition period. All inductors are coupled and wound on a single core which

reduces the size, weight and cost. But the combination logic of circuit causes higher peak current on main switches during transition. The transient, dynamic performances are enhanced and efficiency is increased by the reduction of ripple current and switching losses. The synchronous interleaved high gain converter [20] reduces the ripple content on source current by conventional ripple cancellation scheme. Also the zero voltage switching is achieved for all four switches by the circuit of soft-switching cell. Additional coupled inductor along with extra dc link capacitor circuit is used to achieve soft switching. A high step-up converter with interleaved circuits [21] increases the voltage gain by multiplier capacitor circuit. The zero voltage transition is achieved by capacitor connected across the switch. Each interleaved circuits consists of three winding coupled inductor which reduces the ripple content on source current. The circuit consists of large number of inductors and capacitors makes a challenging dynamic performance. Even if the converter size and weight are larger but the reduction of losses increases the efficiency to high. The soft switching of interleaved converter achieved by connecting snubber circuit with auxiliary switch in the reported manuscripts [22]-[23]. The main switches are operated by zero voltage transitions and auxiliary by zero current turn on and zero voltage turn off. The elimination of switching losses improves the efficiency of interleaved step-up converter in continuous conduction mode (CCM). The additional circuits to achieve zero power transition causes increased size, delay in response, complex analysis and also result in increased cost.

A simple step-up interleaved circuit [24] reduces the source current ripple and the output voltage is improved by diode-capacitor multiplier circuit. The combination of the multiplier circuit is inserted in each interleaved circuit to improve the voltage gain. The ripple content is further reduced by mutliphase interleaved circuits and large step-up

gain is achieved by n number of multiplier circuits. Also the gain of the circuit is improved further by cascade of third level boost circuit [25] along with multiplier circuit. The additional switches with capacitors in the circuit for high step-up gain reduces the voltage stress of the interleaved switches. A dual input interleaved circuit[26] increases the voltage gain to high. The voltage gain is improved by diode-capacitor multiplier circuit. The converter can be utilized along with two generating sources like solar and fuel cell. Also the converter yields good efficiency due to trim down of losses by ripple reduction.

The current stress of the switches are reduced by semi active quadrupler converter in interleaved step-up circuit shown in the paper [27]. The voltage doubler circuits along with combination of phase shift and conventional PWM scheme are utilized to obtain higher gain. The isolated converter with capacitor connected across the switches to achieve soft transition of transistors.The secondary side of the transformer is formed as a rectifier with semi active circuit to reduce conduction losses. Though the converter system having more number of components and larger size, it provides good efficiency. The simple interleaved step-up circuit alternative phase shift and interleaving PWM control [28] controls the source current. The input current and output voltage are sensed to deduce the new PWM scheme by the combination of aforementioned switching logic suitable for duty ratio less than and equal to 0.5. The output gain is improved by diode-capacitor voltage multiplier circuits suitable for fuel cell generation systems. The switching scheme adopted decreases the switching voltage stress through out light and high loads.

The coupled series inductor with capacitor multiplier circuit [29] improves the voltage gain of the interleaved converter circuit many times and can be utilized with renewable energy systems. The input side is connected with two parallel additional coupled inductor circuit to achieve trimming of ripple content of source current. The

switched capacitor circuit makes the dynamic characteristics of the circuit challenging. Also the circuit becomes bulky and in larger size due the multiple number of coupled inductors. A high gain step-up multiple phase interleaved converter with modular circuits [30] suitable for wind farms analyses the challenges with high power converters. The secondary side of the isolated modular converter is connected with fault tolerance circuit to provide protection. The reduction in losses improves efficiency but four switches and higher number of inductors in one modular circuit increase the size and weight. of the modular circuit. A special pulse logic control circuit is required to trigger the switching devices. The high voltage gain interleaved circuit [31] suitable for high power applications yields high efficiency with feasibility of isolation, soft switching and modularity. The complex modular converter has rectifier on the output side of the isolation transformer with series coupled inductors. The converter regulates the output voltage tightly which overcomes the challenges of large variation output voltage for small changes of input suitable for high voltage direct current (HVDC) applications. The parallel input series output structure improves the quality of source current and enhances the output voltage in large.

An interleaved converter with floating ground provides high gain using outer robust voltage control and inner sliding mode control in the presented work [32]. The control techniques regulate the converter to constant output voltage and also share the input current equally through the inductors. The control scheme improves the over shoot and settling time of output voltage during transient operations. The controller is insensitive to uncertainties of supply and can be utilized with fuel cell systems. The power loss of the interleaved converter is tabulated against the temperature and found that the reliability of the interleaved structure [33] is high. As temperature increases, power loss is increased, thus reliability decreasing, but is better than

conventional DC-DC boost converters.

2.3 Reduction of Ripple in Step-down Converters

Conventional buck converter operates with high ripple on load current. The interleaved structure with ZVS reported in the paper [34] reduces ripple on load current and regulates the output voltage. The interleaved inductors are coupled and the leakage energy is re-used by clamp circuit and hence the efficiency is improved. By operating the converter at boundary conditions, the zero voltage switching can be achieved by charging and discharging of inductors with the output capacitor without the additional circuitry. The switching transients can be reduced with zero power transitions and dynamic characteristics can be improved. The two phase circuit can generalized with adding interleaved modules to improve the shape of load current further and hence the output voltage. The switches connected in series in interleaved structure of step-down converter [35]-[36] reduce the switch voltage instead of applying soft switching schemes. The conventional circuit is modified by focusing improved step-down ratio along with ripple reduction on output. Also an auxiliary capacitor-diode circuit is added to enhance the performance of the converter under transient conditions. The additional circuitry is not affecting the characteristics of the converter under steady state operating conditions. The series connected switches have to be operated simultaneously by PWM to share the voltage, delay in simultaneous operation causes to transients. The synchronous non-isolated step-down circuit with quasi resonant switching logic [37] improves the converter efficiency. The discontinuous mode and

continuous mode of operations are carried out respectively in light and heavy load conditions to meet the requirement of zero voltage transitions. The control algorithm used along with valley switching logic enables ZVS without any auxiliary circuits improves the output power, hence also the efficiency in discontinuous conduction mode (DCM) of conditions. By eliminating auxiliary components, the converter provides pertinent advantages like compact size, light weight, low cost and in addition, it can be adopted in integrated circuit (IC). The dual control scheme mainly applied in light load conditions and the output voltage increment may cause to change the synchronous voltage across switch and it results into switching losses under heavy load conditions, leads to decrease in efficiency. A step down converter with high gain circuit with dual series circuit [38] reduces the voltage stress of the switches and increases the efficiency to high. Due to the connection of capacitors the input voltage is not equally shared between two interleaved circuits but the same capacitors shares the output current is equally in inductors with the aid of additional switch. The same duty ratio on two phases of the interleaved circuit provides twice the current in one of the interleaved circuit. To balance and share the current equally in each phase of the interleaved circuit, the duty ratio of the switches is made different. This results into unbalanced step down conversion ratio of voltages in each phase of the interleaved circuit. This circuit is applicable to tightly regulated output voltage under frequent transients and where high step down conversion ratio required with extremely higher input voltage.

A simple buck converter with the combination controller of fuzzy and proportional integral derivative (PID) [39] in closed loop voltage mode control improves the dynamic performance of the converter. The synchronous buck converter is triggered by digital PWM (DPWM) which is generated with fuzzy logic and PID controller.

The combination controller reduces the hardware cost of the closed loop control in comparison with other superior controllers. The dynamic behavior of parallel step-down converter [40] is investigated and the instabilities are mitigated by master-slave closed loop control. The stability of the parallel converter is verified by bifurcation analysis by considering the new variable as phase shift.The transient instability is suppressed by optimal resonant perturbation and the load current is equally shared by output voltage mode master slave control.

A three level interleaved buck converter presented [41] - [42] with dual high voltage inputs operates at zero voltage transitions for all controlled switches. The isolated converter consists of two circuit modules operated by the switching logic of two phase PWM. Each module has double three level circuits with many number switches and secondary side output of the transformer is rectified by diodes which is also under soft switching of zero current. The complex interleaved circuit is triggered by PWM schematic reduces the voltage ripple on output side and shares the load current. The hybrid converter balances the two input voltage source and clamp voltage across the switch to half of the input voltage. The output ripple current is reduced by rectifier with current doubler circuit. More number of inductors causes to a heavy circuit in larger size and a crucial dynamic behavior due to more number of switches. A four phase step down converter reported in the paper [43] shapes the output voltage to a steady DC by eliminating ripple content. Automatic current sharing feature balances the output current and reduces the voltage stress of the switches to half and diodes to one-fourth of supply voltage respectively. The circuit resembles to three level converter and suitable for applications with high input voltage with high efficiency. The efficiency of the converter is further improved by replacing diodes with MOSFETs. In a four phase

converter the duty ratio is limited 0.25 with special PWM logic to trigger the converter switches. The extension of duty ratio increases the voltage stress of the devices to input voltage.

A generalised circuit interleaved four phase converter with DC blocking capacitors [44] diminishes the voltage stress of controlled and uncontrolled switches. The voltage across the blocking capacitor in the circuit varies accordingly the rise and fall of the input voltage, hence the voltage across the switches are controlled. The charge balance of capacitors shares the current uniformly through the interleaved phases. The phase shifted PWM logic applied to switches reduces the current considerably. The added inductor [45] on output side further reduces the ripple content of load current. Also this converter reduces the voltage stress of the switches to one fourth of the source voltage. The additional switched capacitors on each phase challenges the dynamic behavior of the converter and more number inductors causes to higher size and weight. The stability of the converter is to examined with one the well known conventional control scheme.

The autotuning algorithm in an interleaved synchronous step-down converters presented in the papers [46] - [47] shares the current equally between the phases without the usage of same number of sensors. The input voltage ripple difference of two phases is minimized within a cycle in two phase converter by the controller, while keeping tight regulation on output voltage. The sensed output voltage is fed to a two pole compensator and the error processed by autotuning sensorless logic to yield PWM pulses for switches. Finally the algorithm is extended to more number of phases for equal current sharing and it saves cost and reduces size of the converter. The main switches of interleaved step down converter is operated by zero voltage transition along with an auxiliary circuit [48]. The additional auxiliary circuit consists inductors, diodes and capacitor

and switch cause more complexity in circuit and also the auxiliary switch is operated by zero current switching. The reduction of ripple on output voltage and switching losses improve the efficiency of the converter. The additional inductors in circuit and zero voltage transition improve the transient and dynamic performance of the converter. The switching logic scheme to trigger the devices is generated by phase shift control suitable to interleaved converters. The load power is driven from two sources such as renewable source and battery in an interleaved three port converter [49]. The interleaved structure reduces the filter size on the output and ZVS technique reduces switching losses. The additional coupled inductors and input capacitors in the three port system add up the complexity along with large weight and size. The conduction losses and switching losses are trimmed down in isolated full bridge converter [50]. The circulating currents are eliminated by phase shift control with zero voltage transition in secondary side. The high power circuit is designed with high frequency transformer and a rectifier suitable for fuel cell systems.

The number of inductors in a converter increases size and weight of the overall module. If two inductors are coupled in single core which reduces the size of the converter. Size and compatibility are major issue in converters which are used in servers, memory units, new generation computer processors etc.. An interleaved step-down converter designed by considering coupling effect in the paper [51] to avoid the early saturation of inductor current. Also the paper investigates the interference between phases in the physical design by evaluating coupling coefficient using equivalent reluctance models. When two inductors are directly coupled with very short coupling distance, if one of the inductor is discharging and the other is charging then there is abrupt change in the slope of first inductor during the short period of interference and it comes to the normal

state after a small interval of interference. This distortions affect to ripple building and cause for losses which reduce the efficiency. An indirect coupling of inductors in very short distance is one of the solution suggested to reduce the slope of inductor discharge.

A compact inductor winding structure in interleaved synchronous step-down converter [52] reduces the space and size of the circuit module and it can be utilized in sophisticated equipments like laptops, mobile etc.. The design of the converter is carried out at high switching frequency and the selected indirect coupling reduces the ripple associated losses and improves the efficiency of the converter. As the distance between winding increases, the coupling coefficient decreases, the dimensions of the core is decided based on the surface area available in the PCB and the distance of the winding fixed by selecting suitable type of coupling.

Step-down and step-up operations are carried out using a bidirectional converter with interphase transformer in the paper [53]. The switches of the interleaved structure are operated by complementary pulses with same duty ratio which reduces the voltage stress. The inductance mismatch in interleaved converters in the reported paper[54] cause to vanish the advantages of low ripple and reduction of voltage stress across switches. The ripple cancellation is not carried out if there is difference in inductor values, it causes of harmonics on AC side, which increases THD. The ripple current equation is characterized in terms of duty cycle and it allows one to evaluate theoretically the performance of the ripple associated expressions without the software or hardware validations of the converter circuit. This easiness can lead to moderate optimizations of inductor values in interleaved converters. The assumption of constraints to characterize the total ripple may cause to an approximate analysis and it results in to variations in actual ripple values.

2.4 Impact on Power Quality by Basic Circuits of Buckboost Converters

The high voltage gain of the buckboost converter [55] and trimming down of conduction losses improve the efficiency and hence the performance improvement. The voltage stress of the switch and diodes reduced by the connection of additional capacitor. A single inductor buckboost converter [56] regulates output voltage tightly against wide input voltage and load current variations with high efficiency. By using time multiplexing logic, auto allocation of buck or boost mode is enabled which resolves the issue of unbalanced loadings on different channels. The control algorithm of first order converter in closed loop operation enables the converter to settle fast and hence improves the transient behaviour against wide output changes.

The interleaved buckboost circuit with inversely connected coupled inductor [57] with ZVS improves the dynamic characteristics. The current control in critical mode reduces the volume of the magnetics along with inversely connected coupling of inductors. The switching losses are reduced by ZVS, which improves the efficiency and also the converter transient performance is improved by current sensing control scheme.

The output voltage of the buckboost converter with non-inverting output and interleaved structure suggested in the paper [58] improves converter conversion efficiency by reducing current ripple at low voltage when operated at high power. This converter suggests a solution to the problems related to differential ground in buckboost converters, also reduces cost by eliminating some of components which improves transient performance. An interleaved step-up module integrated with buckboost converter and isolation

transformer [59] deduced from analysis of the basic converter topologies to conduct the DC - DC conversion effectively with high efficiency. The integrated converter yields better steady state characteristics even with more number of components and diode capacitor multiplier circuit. The step-up of the voltage is conducted by multiplier circuit and it reduces the turns ratio of the high frequency transformer, also multiplier circuit provide the advantages of reduced conduction loss and reduced voltage stress across semiconductor devices. The integrated converter components make a challenging dynamic and transient behaviour and also zero voltage switching to be employed to improve the characteristics during transition. The DC - DC converter with hard switching generally used in low power circuit, but in high power circuit zero power transition of switch is utilized to decrease switching losses. A flyback converter half bridge interleaved circuit [60] with zero power transition in switches reduces the switching losses and improve the efficiency. The switches in converter with coupled inductors turned ON at zero current and turned OFF at zero voltage. The complex circuit with more number of inductors make the circuilt larger and but the dynamic behaviour of the converter is improved. An isolated flyback interleaved converter with ZVS [61] reduces the switching and conduction losses to improve the efficiency. The PWM scheme for the dual switches is generated by using input current and output voltage sensors with three compensators in a digital controller. The auxiliary inductors and two transformers integrated in the circuit cause to larger and weightier topology.

The boost voltage output of the Single Ended Primary Inductor Converter (SEPIC) topology recommended in the paper [62] provides high gain with reduced switch stress by an additional clamping circuit. The cascaded SEPIC circuit provides a smooth input current with zero ripple by the aid of an auxiliary circuit in the boost

module and high boost gain by the help of more turns ratio in coupled inductor. Reduced switch stress allows the selection low rating MOSFET which reduces conduction loss hence efficiency of the system increased. The limitation of the converter the high gain conversion is applied only for boost operation. Also the coupled inductor, ripple reduction circuit, auxiliary circuit etc. increase the size, weight, cost and make analysis complex during trouble shooting stage. The dynamic characteristics of the DC-DC SEPIC topology [63] is analyzed using modal analysis by forming analytical expression for transient conditions. The non-linear modal analysis with large disturbance yields optimal design suitable for better transient characteristics by the help of correlation of state variables and also suggests interactions with second order transfer function is much stronger in non-leading oscillations The SEPIC circuit with interleaved structure [64] operates transition of switches in ZVS scheme for the duty cycle above 0.5 and reduces switching losses. But when the converter operated below 0.5 duty ratio the switching losses are predominant at high frequencies. The ZVS scheme is executed with resonant inductor connected in series with Drain terminals of the MOSFET. The SEPIC topology with energy storage circuit [65] can be utilized for multiple inputs with energy generating systems. The converter consists combination of bidirectional and unidirectional ports to receive the power from the source and to charge the battery also. The circuit consists of three switches for two input systems requires a special switching logic and the increase in number of switches with number of sources make the dynamic behavior of the system critical with increased cost. The ripple on output voltage and the equation for switch peak current is derived in SEPIC circuit [66] in CCM. The design of input inductor, the magnitude in source voltage and the load current decide the peak current of switch and the values of output inductance and capacitance determine ripple on load voltage.

A Cuk converter with Hysteresis controller in CCM [67] and DCM [68] are analysed to generate PWM switching logic. The stability of the converter system is verified with Lyapunov function represented as semi-definite expressions. The matrix inequalities in linear mode are used to evaluate Lyapunov quadratic equations. The control law improves the transient and dynamic characteristics of Cuk converter.

2.5 Power Quality Improvement

The snubber circuit along with interleaved step-up converter is suggested in the paper[69] to achieve ZVS for controlled switches and ZCS for diodes. The input side of the converter is a rectifier, the parallel PWM scheme selected cancels the ripple on source current and also improves the output voltage. The converter is operated in closed loop with current control, that shapes the source current, reduces THD and improves the power factor. The soft switching is achieved with an expense of additional circuit with isolation transformer leads increased size, weight and cost. The interleaved stepdown converter with current mode control using slope compensation [70] technique reduce THD and power factor of input AC source. The AC input side is connected with capacitive - inductive - capacitive (C-L-C) filter with coupled inductor to shape the input current and rectifier output is connected also with another C-L-C filter to derive stiff DC voltage suitable for interleaved converter. The output current is sensed for phase management to control the dynamic performance at light load conditions. The input voltage is sensed by feed forward scheme to improve factors of the slope compensation and current clamping circuit is used to control the power factor to high for large input voltage variations. The generation of PWM logic with the complex control circuitry requires

a high end processor to evaluate composite algorithm which increases the overall cost of the total converter system.

The two stage converter with interleaved transformer [71] improves the power factor of the circuit by sharing the current. The converter operates with high number of switches, interleaved transformer, coupled inductors and switched capacitors make the circuit complex and a special derived switching logic is essential. The basic buckboost converter consists of inductor neither on input side nor on output side and hence the power factor becomes poor when it is connected to AC source through rectifier. An interleaved boost cascaded with buckboost converter is put forward in the paper [72] to reduce DC source side ripple and hence to reduce THD on AC side. This converter is one of the basic circuit to improve the power factor and also reduces the voltage stress with enhanced efficiency. The SEPIC interleaved converter in DCM [73] regulate the power factor by the coupled inductor circuit. The converter is operated in DCM to get better stability and to achieve ZVS transition for the controlled switches and ZCS transition for uncontrolled switches. As the output voltage across DC link varies widely but the power factor is tightly regulated. The operation of the converter is limited to DCM of current since the converter in CCM causes for large switching losses which reduces the overall efficiency.

An inductive - capacitive - inductive (LCL) filter is used in bidirectional converter [74] - [75] to achieve zero power transition in the semiconductor devices. The resonant network with voltage doubler by series capacitors increases the converter voltage gain in boost mode without the isolation transformer. The step down conversion on the other direction is also increased by decreasing the voltage to half by equal capacitor division. The reduction in voltage and the complimentary PWM logic decreases the switch stress. The high frequency operation of the converter reduces the size and weight

of the inductors and ZVS increases the efficiency. The analysis of the converter is complex and challenging due to multiple equations for buck and boost individually along with resonant parameters.

The droop control scheme is presented [76] to provide a solution to the second harmonic ripple across DC voltage controller for a single phase inverter with LCL filter connected to the grid. The control scheme eliminates the voltage component with twice the frequency from the DC bus voltage and prevents the ripple component flow to the current control loop and to the grid. Hence the third harmonic distortion is reduced and the filter size is considerably decreased to enhance THD and to improve power factor. The relevant features of a few of the converters are summarized in tabular form in the Table 2.1. The review of the converter can be summarized as follows.

2.6 Summary

The input side inductor of interleaved boost converter [9] - [18] shares the source current and improves the shape but the output current is pulsed. The auxiliary resonant circuits to reduce switching losses, voltage multiplier and switched capacitor circuits [19] - [33] to improve voltage gain, result into complex trouble shooting analysis, Also the inductor on output side decreases ripple on load current in buck converters [34]- [54], but the source current is pulsed. The source and load currents of the circuits with buckboost topologies [55]-[61], are pulsed due to the absence of inductors either on input or output sides. The inductors present on both sides of SEPIC and Cuk converters [62]-[68] reduce the source and load current ripples which improves the quality AC source current to certain extent.

If a DC-DC converter is required to be operated for high currents

Table 2.1: Issues related to DC - DC Converters

Converter	Merits	Issues
Boost	Source current is continuous, Gain improvement	Pulsed output currents Switched capacitor
Buck	Output current is continuous Wide duty ratio	Pulsed current on source side Large switch stress
Buckboost	Step down and step up Wide variation of duty ratio	Pulsed currents on input and output Poor transient behavior
SEPIC, Cuk	Continuous current Buck and boost operation	High switch stress More settling time, overshoot
Interleaved	Low switch stress, Parallel outputs Duty ratio < 0.5	Multiple switches, Parallel outputs same magnitude Limitation on output

then sharing of currents reduce the size of components. In such cases interleaved converter is viable option not only to share the source current but also to reduce the ripple on source current. The power quality of the converter is verified by connecting it to AC source with a rectifier circuit. An optimum filter circuit [69] -[71] is used along with various topologies [72] - [76] to reduce THD and hence the power factor. The significant issues to be addressed while operating DC - DC converters are ripple current, high switching stress, number of outputs, regulation, switching losses, oscillations on output and transient behavior. The proposed topologies to address the above issues are extensively analyzed and effectively validated in the coming chapters.

Chapter 3

Conventional Cuk Converter

3.1 Introduction

Conventional Cuk Converter (CCC) [4] is a DC to DC converter which delivers an output voltage higher or lower than the input voltage. Also the output has the polarity opposite to that of input voltage. As against the well known Buck boost converter, which provides pulsed current on both input and output sides, the Cuk converter provides continuous currents on both sides. The output voltage equation is similar to that of the Buck boost converter. The circuit diagram of an ideal cuk converter is shown in Fig.3.1.

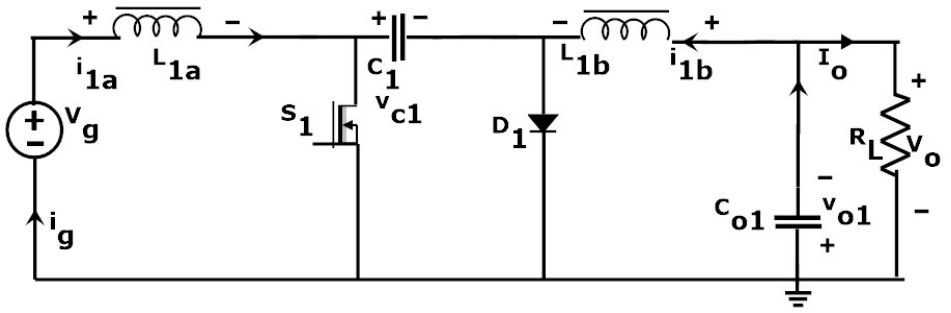


Fig. 3.1: The circuit diagram of CCC

The circuit consists of input inductor L_{1a}, filter inductor L_{1b}, energy storage capacitor C_1, filter capacitor C_{o1}, input source V_g, load resistance R_L, switch S_1 and diode D_1. The input voltage V_g is applied produces the output voltage V_o measured across load resistance R_L. The input and output inductors ensure the delivery of continuous currents on both sides.

The operation of the converter is based on capacitor energy transfer, the capacitor C_1 acts as primary means of storing and transferring energy from the input to the output. The average inductor voltages V_{L1a} and V_{L1b} are zero at steady state. The capacitor C_1 is designed in such a way that it transfers the constant voltage. The circuit has low switching losses and high efficiency. The converter operation is explained in two modes as given below.

3.2 Modes of Operation

The converter transfers the input power to output power by operating it in two states. The first state is when the switch S_1 is in

ON position and the second state is when the switch S_1 is in OFF position. The energy storage element C_1 stores energy during OFF state of switch and transfers to output during ON state of switch. The modes of operation are mentioned as Mode-1 and Mode-2 and is explained below.

3.2.1 Mode -1 : Switch S_1 in ON state

The ON state circuit diagram is shown in Fig.3.2. The inductors L_{1a}& L_{1b} get energised and capacitors C_1 & C_{o1} are discharged when the switch S_1 is closed. The load current is assumed constant and flows in negative direction as shown in Fig. 3.2. The inductor L_{1a}

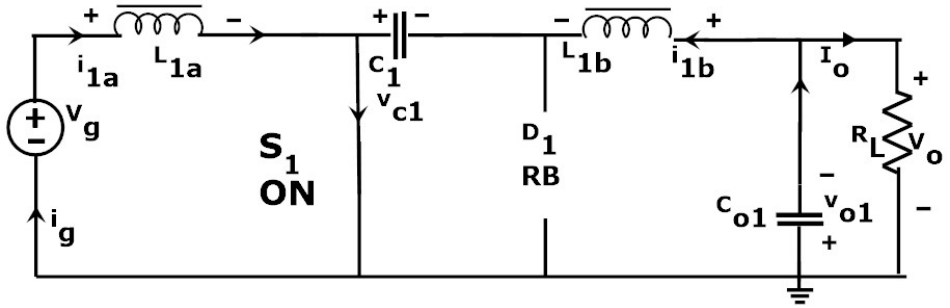


Fig. 3.2: Circuit diagram of ideal CCC when the switch S_1 is ON. (D_1 RB - Diode in Reverse Bias)

is energized and capacitor C_1 reverse biases diode D_1. Therefore C_1 discharges its energy through C_1, C_{o1}, L_{1b} and through the load R_L.

The charging and discharging of inductor currents and capacitor voltage are shown in Fig.3.3. . During $t_{ON} = dT_s$ period, where d = duty cycle, $0 < \mathrm{d} < 1$ and T_s switching period, inductor current rises from initial value I_1 and reaches to peak value I_2. At t = t_1, the

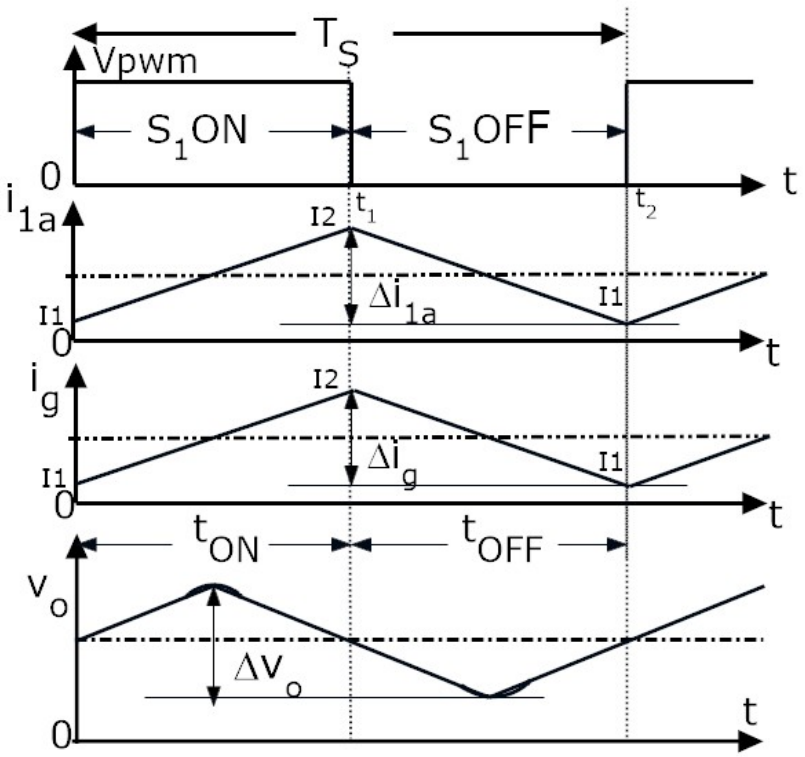


Fig. 3.3: The inductor current and output capacitor voltage waveforms

switch S_1 opens and inductor starts discharging. The capacitor C_1 discharges and transfers its previously charged energy to load. The capacitor C_{o1} filters ripple on output voltage and the inductor L_{1b} is getting charged.

By assuming linear rise of inductor current, ripple current ΔI_1, during Mode-1 is given by Eqn. (3.1).

$$\Delta I_1 = t_{ON} V_g / L_{1a} \tag{3.1}$$

Where V_g is the input voltage. Obviously, the ripple on inductor current in Mode-1 depends on pulse width of ON time, inductor value and input voltage.

3.2.2 Mode -2 : Switch S_1 in OFF state

The circuit diagram with switch S_1 in OFF state is shown in Fig. 3.4. At the instant t_1 switch opens and inductor starts discharging during

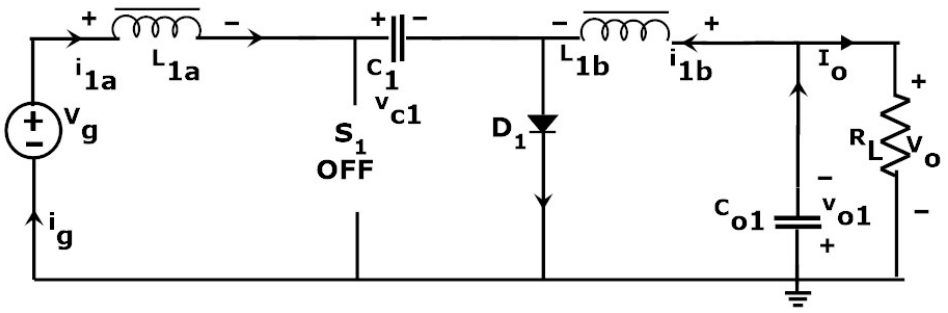


Fig. 3.4: Circuit diagram of ideal CCC when the switch S_1 is OFF state

the period $t_{OFF} = (1-d)T_s$. At t_2 it reaches to initial value I_1 and switch closes. When the switch S_1 is opened, the inductors L_{1a}, L_{1b} are discharged and capacitors C_1, C_{o1} are charged with the diode D_1 closed naturally. The load current I_o is assumed constant and flows in the negative direction, towards R_L. The element C_1 charges from input power supply and energy stored in L_{1b} charges up the capacitor C_{o1}. By assuming linear fall of inductor current, the ripple current ΔI_1 is given by Eqn. 3.2), (referring to Fig. 3.3)

$$\Delta I_1 = -t_{OFF}(V_g - V_{c1})/L_{1a} \tag{3.2}$$

Comparing equations (3.1) and (3.2), V_{c1} can be expressed as

$$V_{c1} = V_g/(1-d) \tag{3.3}$$

where $d = t_{ON}/(t_{ON} + t_{OFF})$ Also assuming that the inductor current in L_{1b} rises linearly during time t_{ON} and falls linearly during t_{OFF}, during t_{ON}, ΔI_2 can be expressed as

$$\Delta I_2 = (V_{c1} + V_o)t_{ON}/(L_{1b}) \tag{3.4}$$

Similarly during t_{OFF} the ripple current, ΔI_2

$$\Delta I_2 = -t_{OFF} * V_o/L_{1b} \tag{3.5}$$

From equations 3.4 and 3.5, it can be deduced that

$$V_o = -V_{c1} * (t_{ON}/(t_{ON} + t_{OFF})) = -V_{c1} * d \tag{3.6}$$

Substituting Eqn. (3.3) in Eqn.(3.6), the output can be given in terms of V_g as Eqn. (3.7),

$$V_o = -V_g(d/(1-d)) \tag{3.7}$$

Output Current for resistive load R_L is given by the Eqn. (3.8)

$$I_o = V_o/R \tag{3.8}$$

Thus it turns out that the output voltage can be varied by changing duty ratio of switch, by keeping input voltage constant. The duty ratio can be varied by changing the ON time of Pulse Width Modulation (PWM) by keeping time period constant. By comparing triangular carrier wave with DC signal in the case of PWM, the on time and hence the duty ratio d can be varied.

The design of a power supply system is often stable, providing sufficient amount of gain and phase margins over a wide range of

frequencies. The designs also show zero steady state error. However, the transient responses often leads to large amount of unwanted ringing and over shoots, where there is much room for improvement. The feedback compensation then suggests itself as the right choice for the said improvement. The motivation behind the feedback control is to shape the open loop gain of the system, so at to achieve low steady state error. Among the many techniques available for compensation, the dominant Pole Compensation is by far the simplest and most common form of feedback compensation. The open loop transfer function of the plant is therefore required to effectively implement the feed back scheme

3.3 Derivation of Transfer Function from State Space Model for Open Loop Plant of CCC

Following the classical model of the linear system using the state space theory, the transfer unction of a system is given by

$$G(s) = C * (sI - A)^{-1} + E \tag{3.9}$$

where the system is modelled as

$$\frac{dx(t)}{dt} = A * x(t) + B * u(t) \tag{3.10}$$

and

$$y(t) = C * x(t) + Eu(t) \tag{3.11}$$

The state is given by

$$\begin{bmatrix} x(t) \end{bmatrix} = \begin{bmatrix} i_{1a}(t) & i_{1b}(t) & v_{c1}(t) & v_{o1}(t) \end{bmatrix}^{\mathrm{T}}$$

where the state variables are
$i_{1a}(t)$, current through inductor L_{1a}
$i_{1b}(t)$, current through inductor L_{1b}
$v_{c1}(t)$, voltage across capacitor C_1 and
$v_{o1}(t)$ voltage across output capacitor C_{o1}.

The output y(t) is given by

$$\left[\ y(t)\ \right] = \left[\begin{array}{c} i_g(t) \\ v_o(t) \end{array}\right]$$

where
$i_g(t)$, current through the the source and
$v_o(t)$, voltage across load resistance.

The state space modelling of practical CCC in terms of the above state variables is discussed in detail in Appendix A.1.

The state space modelling of practical CCC is shown in Appendix A.1. From state space model of Appendix A.1, the state matrices A,B, C and E are given below as,

$$A = d * A_1 + d' * A_2 \tag{3.12}$$

$$B = d * B_1 + d' * B_2 \tag{3.13}$$

$$C_{mod2R_2} C_{stateR_1} = d * C_{mod1R_1} + d' * C_{mod2R_1} \tag{3.14}$$

$$C_{stateR_2} = d * C_{mod1R_2} + d' * C_{mod2R_2} \tag{3.15}$$

where d' = 1 - d, C_{stateR_1} and C_{stateR_2} are first and second rows of output C matrix. Applying small perturbations $\hat{x}(t)$, $\hat{u}(t)$ and $\hat{d}(t)$ in time domain respective functions $x(t), u(t)$ and in $d(t)$, then the small signal ac model [77] is given in equations 3.16 and 3.17.

$$\frac{d\hat{x}(t)}{dt} = A\hat{x}(t) + B\hat{u}(t) + ((A_1 - A_2)X + (B_1 - B_2)U) * \hat{d}(t) \quad (3.16)$$

where X denotes the state variable in steady state

$$\begin{bmatrix} X \end{bmatrix} = \begin{bmatrix} I_{1a} & I_{1b} & V_{c1} & V_{o1} \end{bmatrix}^{\mathrm{T}}$$

and U = V_g. The output is given by

$$\hat{y}(t) = C\hat{x}(t) \quad (3.17)$$

In this converter $B_1 = B_2$, so $B_1 - B_2 = 0$, E_1 =$E_2 = 0$
and hence the solution in s domain is given by

$$\hat{x}(s) = (sI - A)^{-1}B\hat{u}(s) + (sI - A)^{-1}(A_1 - A_2)X * \hat{d}(s) \quad (3.18)$$

The output is given by

$$\hat{y}(s) = C(sI - A)^{-1}B\hat{u}(s) + C(sI - A)^{-1}(A_1 - A_2)X * \hat{d}(s) \quad (3.19)$$

Accordingly, the output voltage is given by

$$\hat{v}_o(s) = C(sI - A)^{-1}B\hat{u}(s) + C(sI - A)^{-1}(A_1 - A_2)X * \hat{d}(s) \quad (3.20)$$

Then the transfer function is

$$G_p(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = C(sI - A)^{-1}B\frac{\hat{u}(s)}{\hat{d}(s)} + C(sI - A)^{-1}(A_1 - A_2)X \quad (3.21)$$

The plant transfer function is obtained by keeping the input as constant, that is the variation $\hat{u}(s) = 0$ so

$$G_p(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = C(sI - A)^{-1}(A_1 - A_2)X \tag{3.22}$$

where A_1 - A_2 =

$$\begin{bmatrix} r_{c1} & 0 & 1 & 0 \\ 0 & -r_{c1} & 1 & 0 \\ -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

3.4 Design of Components

A typical design of CCC is now given in detail, addressing all aspects including the selection of components, design of components, detailed design and hardware simulation. The components, L_{1a}, L_{1b}, C_1 and C_{o1} of CCC are designed [4] for -40V, 80W output as given below.

3.4.1 Design of Inductor

Referring to Fig.3.1, the inductor values are designed for an input voltage V_g of 20V and an output voltage V_o of -40V. using the following steps:

1. Calculate the duty ratio d from equation (3.7)
   40=$\frac{20 * d}{1 - d}$, the value of obtained=0.67.
   The load current is limited to -2A due to limitations of laboratory set-up.

2. The load resistance is R_L=$-40/-2$ =20 Ω.
3. The rated output power is -40*-2 = 80W.
4. The source current for 80W power is $80/V_g$ =4A. 20% ripple on input current= 10*4/100 =0.8A. is assumed. Assume the switching frequency f_s as 25 kHz.
5. The inductor value $L_{1a} = \dfrac{20 * 0.67}{25 * 1000 * 0.8} = 0.67mH.$ using Eqn. (3.1) (corresponding to 20% ripple current)

Chose a large value of L_{1a} for continuous conduction. Hence L_{1a} = 0.75mH.

Using Eqn (3.4) (corresponding to 20% ripple current)
$L_{1b} = \dfrac{20 * 0.67}{25 * 1000 * 0.4} = 1.34mH.$
Here again chose a larger value L_{1b} = 1.5mH.

3.4.2 Design of Capacitor

The capacitor C_{o1} is designed for 1% ripple on output voltage as

1. $C_{o1} = \dfrac{\Delta i_{1b}}{\Delta V_o * 8 * f_s}$

   $C_{o1} = \dfrac{0.4}{8 * 0.4 * 25000} = 5\mu\text{F}$

   Choosing a large value, C_{o1} is taken as 10 μF
2. $C_1 = \dfrac{d^2 V_g}{(1-d) * R_L * \Delta V_{c1} * f_s}$. Here $V_{c1} = V_g - V_o$ = 60V.

   $C_1 = \dfrac{0.67^2 * 20}{0.33 * 20 * 3 * 25000} = 18.1\mu\text{F}$

(Assuming $\Delta V_{c1} = 5\%$ of V_{c1}= 3V)

Larger value of 22 μF is taken for C_1. The designed values of components are tabulated in Table 3.1

Table 3.1: Designed values for CCC

parameter	V_g	V_o	I_o	L_{1a}	L_{1b}
Values	20V	-40V	-2A	0.75mH	1.5mH
parameter	C_1	C_{o1}	R_L	f_s	d
Values	22μF	10μF	20Ω	25kHz	0.43

3.5 Compensator Design

By substituting values from Table 3.1 in the equation (3.22) and simulated in MATLAB , the plant transfer function in open loop is given by

$$G_p(s) = \frac{224.9s^3 + 1.12 * 10^{11}s^2 - 8.15 * 10^{14}s + 8.532 * 10^{18}}{s^4 + 5249s^3 + 1.12 * 10^{12}s + 2.17 * 10^{17}} \quad (3.23)$$

As shown in Fig. 3.9, the compensator as a modulator, is inserted in the feed back path, which senses the voltage from the output for correction. A XILINX SPARTAN - 3AN FPGA board was used for realizing the transfer function. The board has an 8 bit ADC, which accommodates the variation of the control voltage v_c from 0 to 256. Varying the duty ratio d from 0 to 100, the modulator gain is given by

$$G_m(s) = \frac{100 - 0}{256 - 0} = 0.39$$

The overall transfer function is given by

$$G_p G_m(s) = \frac{87.71s^3 + 4.38 * 10^{10}s^2 - 3.2 * 10^{14}s + 3.32 * 10^{18}}{s^4 + 5249s^3 + 1.12 * 10^{12}s + 2.17 * 10^{17}} \quad (3.24)$$

The simulated result of bode plot for transfer function of open loop CCC along with transfer function of modulator as given in Eqn. 3.24, is shown in Fig.3.5. The plot shows a phase margin of 12.9° (at

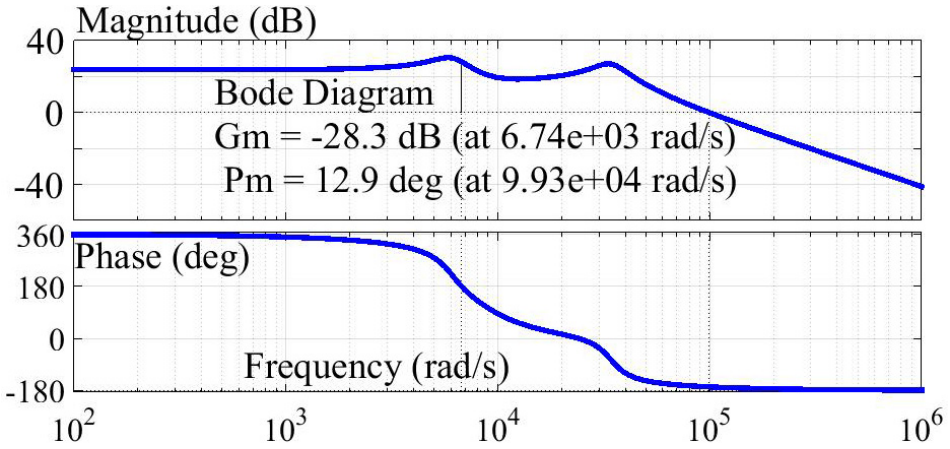


Fig. 3.5: Bode plot of open loop plant with modulator gain of CCC, phase margin =12.9° at $9.93 * 10^4$ rad/sec, gain margin = -28.3 dB at $6.74 * 10^3$ rad/s

a gain crossover frequency of $9.93 * 10^4$ rad/s) and gain margin of -28.3 dB (at a phase cross over frequency of $6.74 * 10^3$ rad/s). The negative value of gain margin and the low value of phase margin suggests the possible instability of the system, which can be corrected by improving phase margin, by using compensators in closed loop. To make the stable operation in closed loop for DC - DC converters, generally compensators of lag, lead or lead-lag designs are commonly utilized.

It is worthwhile to note that phase lag of power converters in general can approach to 180° [78]. In general the phase margin of the system must be higher than 45° for stable operations. When phase margin of the converters fall close to 0°, investigations for uplifting the phase margin is foussed into type I,II or III compensators. Towards this, considering the different types of compensators of Type I, II and III [78] are considered.

It is seen that type I compensator can additionally add another -90° phase lag along with phase lag of feedback loop and it is not meeting the intended purpose, improvement of the phase margin.

On the other hand, though the type II compensator can improve the phase margin up to 90°. In this case the type II compensator can lift the phase lag to 0° at certain frequencies. Accordingly the Type II compensators fall short of the required phase margin. But by focussing to type III compensator it can lift the phase lag above 0° and is considered here as viable option to improve the phase margin.

Looking further into type III compensator, which can give a phase margin boost of additional 90^o. The phase plot is close to -180° at a gain cross over frequency of $9.93 * 10^4$ rad/sec (15.8kHz). As the required phase margin is about 60°, the phase plot has to be lifted up by about 45°. Hence a Type III compensator is utilised in closed loop to take care of the stability.

3.5.1 Design of Type III Compensator

The zeros and poles of the type III compensator is systematically designed to operate the converter into stable operation in closed loop. The design of type III compensator is given in Table 3.2.

Table 3.2: Design of the Compensator for the phase margin ω_m= 12.90^o at the gain cross over frequency of $\omega_{gc} = 9.93 * 10^4 rad/s$ (15.8kHz)

From Fig.3.5, phase margin ω_m= 12.90^o at the gain cross over frequency of $\omega_{gc} = 9.93 * 10^4 rad/s$ (15.8kHz). Therefore
1. $\omega_{p1} = 180 - \omega_m = 167.1^o$
2. $\omega_{p1} = 180 - \omega_m = 167.1^o$,
where ω_m is phase margin. Then
$b = tan(\frac{\omega_{rm} - \omega_{p1}}{2} - \frac{\pi}{4}) = tan(\frac{60 + 167.1}{2} - 45) = 2.56,$
where ω_{rm} is required phase margin
3. Denoting $\sqrt{k} = b + \sqrt{b^2 + 1} = 5.31$
Zeros are given by
$\omega_z = \frac{\omega_m}{\sqrt{k}} = \frac{99300}{5.31} = 18706.3$
poles by
$\omega_p = \omega_m * \sqrt{K} = 99300 * 5.31 = 527282$

The gain crossover frequency, for phase margin ω_m= 12.90^o is $\omega_{gc} = 9.93 * 10^4 rad/s = 15.81$ kHz. The transfer function in general for Type III compensator proposed to be designed is given by

$$G_c(s) = \frac{(s + \omega_Z)^2}{s(s + \omega_P)^2} \tag{3.25}$$

where ω_z and ω_p are arrived at as shown in Table 3.2. Substituting the values of poles and zeroes in equation(3.25) to obtain compensator transfer function,

$$G_c(s) = \frac{(s + 18706.3)^2}{s(s + 527282)^2} = \frac{(s^2 + 2 * 18706.3s + 18706.3^2)}{s(s^2 + 2 * 527282s + 527282^2)} \tag{3.26}$$

The compensator is simulated in MATLAB and the bode plot is shown in Fig. 3.6.

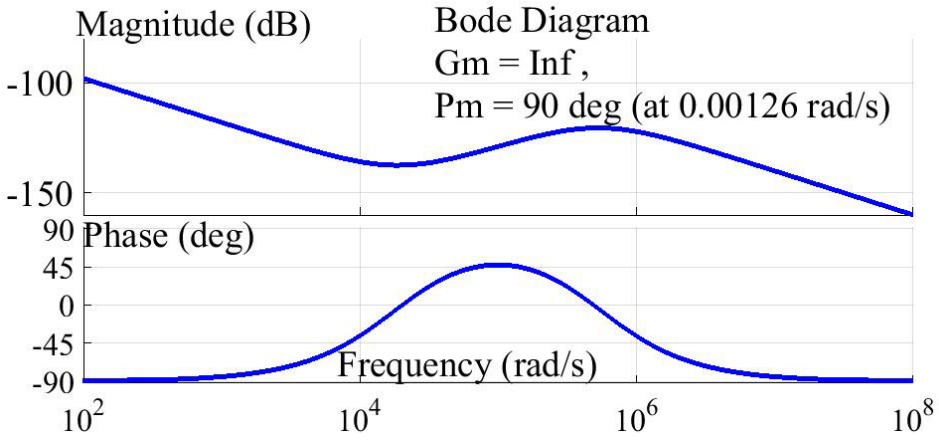


Fig. 3.6: Phase margin = 90^o in Bode plot of compensator without multiplying with gain

Here the gain margin is infinite and the gain plot has to be lifted up by $-120dB$, So
20 log (A) = 120
So the gain is A = 10^6.
Now multilying the compensator transfer function with gain

$$G_c(s) = 10^6 * \frac{(s^2 + 2 * 18706.3s + 18706.3^2)}{s(s^2 + 2 * 527282s + 527282^2)} \tag{3.27}$$

The bode plot of compensator with gain is shown in Fig.3.7.

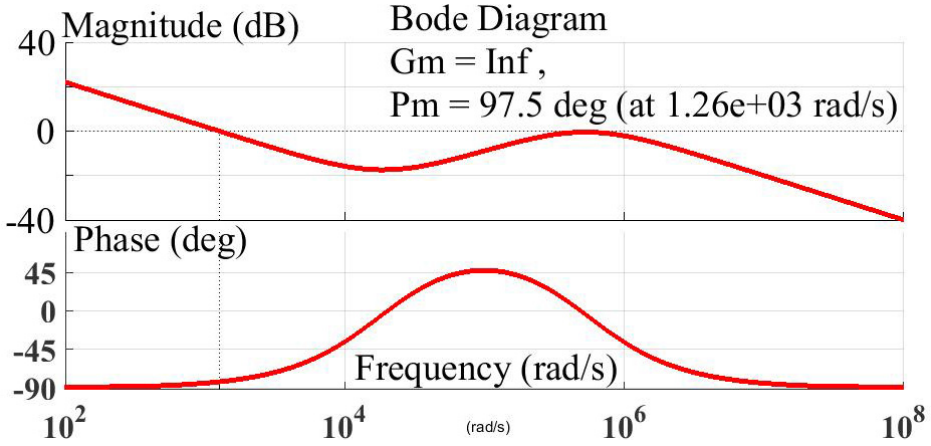


Fig. 3.7: Bode plot of compensator with gain, phase margin = 90^o

From the bode plot the phase margin of the compensator is = 90^o. The overall transfer function, T(s) for the closed loop system with copmensator is obtained by convolution of plant transfer function and compensator transfer function. Now the overall transfer function of the compensated system is given by the Eqn. (3.28),

$$T(s) = G_p(s)G_m(s) * G_c(s) \tag{3.28}$$

$$T(s) = 10^6 * \frac{87.7s^3 + 8.77 * 10^9 s^2 - 6.36 * 10^{13}s + 6.66 * 10^{17}}{s^4 + 13580s^3 + 1.23 * 10^{09}s + 3.07 * 10^{12}} * \frac{s^2 + 2 * 18706.3s + 18706.3^2}{s(s^2 + 2 * 527282s + 527282^2)}$$

The overall transfer function is computed as given by the Eqn. 3.29,

$$T(s) = \frac{(b_2s^5 + b_3s^4 + b_4s^3 + b_5s^2 + b_6s + b_7)}{(s^7 + a_1s^6 + a_2s^5 + a_3s^4 + a_4s^3 + a_5s^2 + a_6s)} \tag{3.29}$$

where $b_2 = 2.63*10^8$, $b_3 = 2.63*10^{16}$, $b_4 = 7.94*10^{20}$, $b_5 = 4.07*10^{24}$, $b_6 = 7.99*10^{27}$, $b_7 = 6.99*10^{32}$, $a_1 = 1.07*10^6$, $a_2 = 2.94*10^{11}$, $a_3 = 5.08*10^{15}$, $a_4 = 3.46*10^{20}$, $a_5 = 9*10^{23}$, $a_6 = 1.21*10^{28}$

The bode plot for the overall transfer function of the copmensated is plotted in MATLAB as shown in Fig.3.8. From the bode plot Fig.3.8

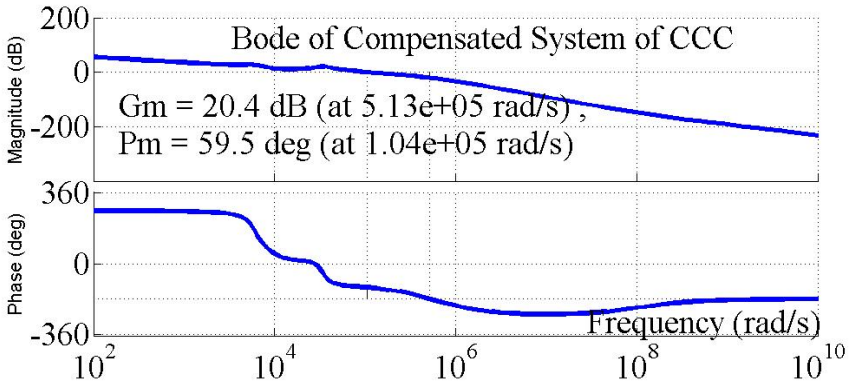


Fig. 3.8: Bode plot of compensated system, from simulated result phase margin and gain margin are 59.5° and 20.4 dB respectively.

the phase margin is 59.5° at a gain cross over frequency of $1.04*10^5$ rad/s and gain margin of 20.4 dB at $5.13*10^5$ rad/s, the compensated system is stable in closed loop. The s-domain compensator in Eqn. 3.27 is converted to z-domain by bilinear transformation [79]. The compensator in z domain is used in XILINX tool of digital FPGA controller for the hardware implementation of the overall system in closed loop. The compensator in z-domain is given in equation(3.30).

$$G_c(z) = 10^9 \frac{3.15z^3 + 9.44z^2 + 9.44z + 3.15}{z^3 + z^2 - z - 1} \tag{3.30}$$

3.6 Simulation Results and Discussion

The CCC, designed as discussed in previous sections, is simulated in closed loop in MATLAB, with the designed values as shown in table 4.1. The simulation has been conducted in open loop and in closed loop for CCC with an input voltage of 20V and output voltage of -40V at -2A and -15V at -2A. The results of closed loop simulation is shown below. The compensator in s-domain is used for closed loop simulation. The closed loop block diagram [80] for simulation of CCC is shown in Fig. 3.9. The corresponding parasitic resistance

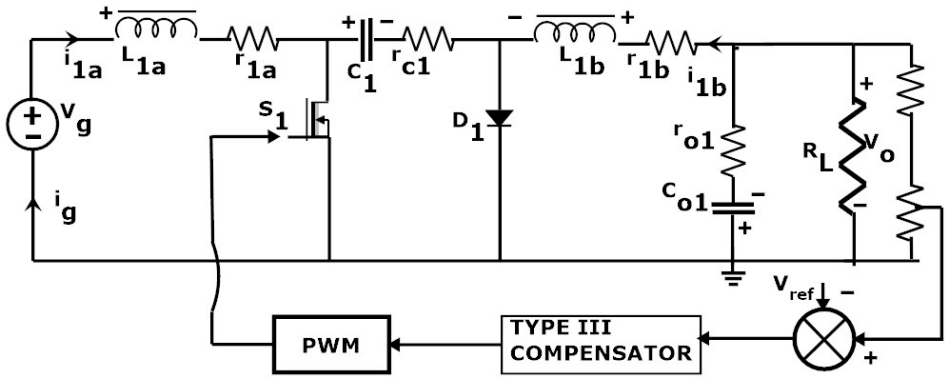


Fig. 3.9: Block diagram for closed loop control of CCC

values of inductors and capacitors need for hardware realization are considered during simulation. The output voltage is fedback and applied to the error amplifier. The error amplifier compares the feedback voltage with applied reference voltage and error is generated. The error is processed in digital compensator which delivers a DC signal for control. This control signal is compared with triangular carrier signal at 25kHz to generate the PWM pulse train, which is used to trigger the switch S_1.

3.7 Closed Loop Operation at an Output Voltage of -15V

With the designed values for -15V,-2A output as shown in Table 3.3, the CCC operates in continuous conduction mode. Both output

Table 3.3: Design values for CCC for -15V, -2A output

parameter	V_g	V_o	I_o	L_{1a}	L_{1b}
Values	20v	-15v	-2A	0.75mH	1.5mH
parameter	C_1	C_{o1}	R_L	f_s	d
Values	22μF	10μF	7.5Ω	25kHz	0.43

voltage and output current are negative and the product is positive hence the converter operates in quadrant III and draws power from the source.

The PWM with duty ratio d = 0.43, is shown in Fig.3.10, at 25 kHz. for switch S_1 (Fig. 3.9). With the input of 20V and output of -15V, the

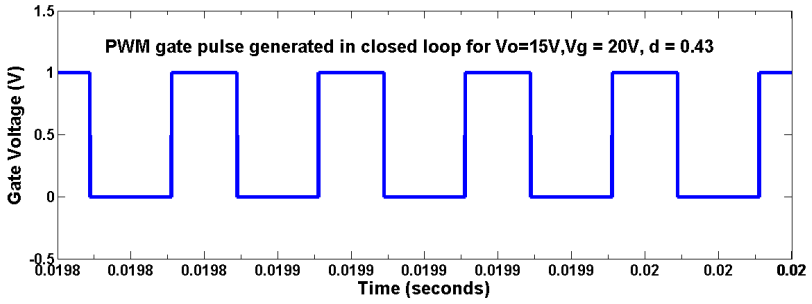


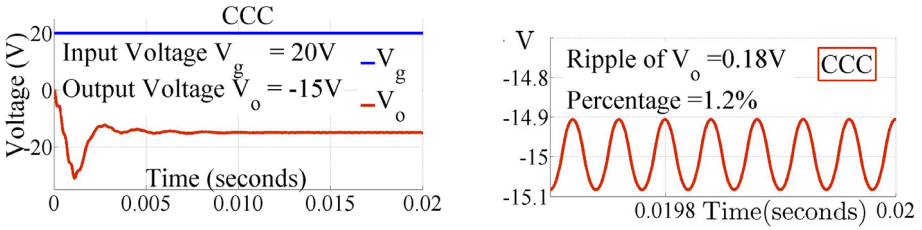
Fig. 3.10: The PWM for CCC to generate -15V,-2A output

duty cycle is evaluated as 0.43 using the output equation (3.7). The

PWM has a period of 40uS and the ON time pulse width is 17.2uS.

3.7.1 Voltage

The output and input voltage of the proposed design of the CCC are shown in Fig.3.11a. It gives a DC output voltage of V_o = -15V with



(a) Voltages of Input V_g =20V and output V_o =-15V **(b)** Ripple on output voltage is 1.2%

Fig. 3.11: Waveforms of CCC at an output of -15V,-2A

V_g =20V DC input. The settling time of the converter is almost 10ms. At the same time the voltage transient is only two times the output voltage. The magnified waveform of output voltage is shown in Fig. 3.11b. The output voltage has a ripple of 0.18V, which is 1.2% of output voltage -15V.

3.7.2 Current

The input and output current waveforms along with their ripples are shown in Fig.3.12. The average value of input current is 1.65A for average value of output current of -2A. The ripple on input current is 0.45A, which is nearly 27% of DC source current. It may be noted that the CCC provides negative output current hence it is plotted in

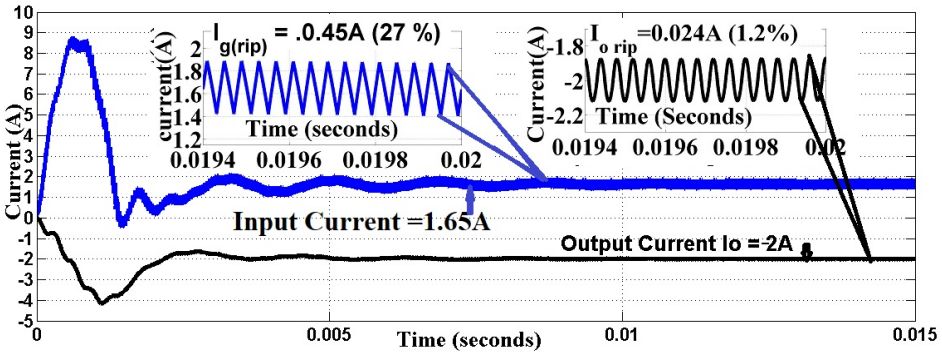


Fig. 3.12: The input and output current waveform of CCC $I_g = 1.65A$ and $I_o = 2A$ for -15V,-2A output.
Ripple on Input current $I_{g(rip)} = 0.45A$.
Ripple on output current $I_o(rip) = 0.024A$

quadrant III in Fig.3.12. With a resistance of 7.5 ohm at the output, the required output current is -15/7.5 = -2A and the value obtained is -2A, which has a ripple content of 0.024A (1.2% of output current).

3.7.3 Transients

The transient response of the CCC for a change of line voltage V_g from 17V to 23V at 30 ms as shown in Fig. 3.13. It can be seen that the output voltage settles back to -15V with a settling time of 30ms. The load transient is shown in Fig.3.14 where load current is changed from -1A to -2A and back to -1A at 15ms and 30ms respectively. The output voltage settles to V_o to -15V, at $I_o = -2A$ with a settling time of 7mS. It is thus confirmed that the CCC is able to stabilize effectively, both against the changes in input voltage and output current.

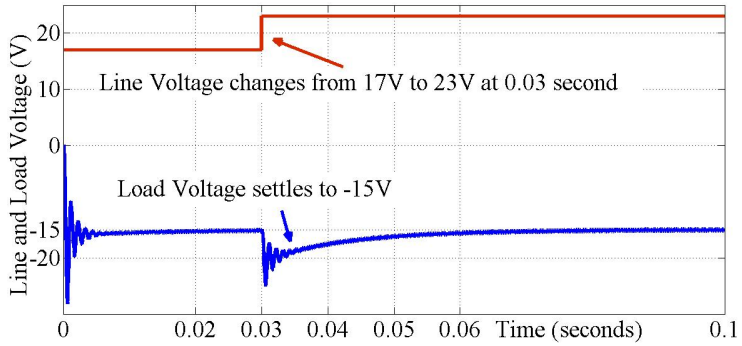


Fig. 3.13: Line transient of CCC for -15V, -2A output

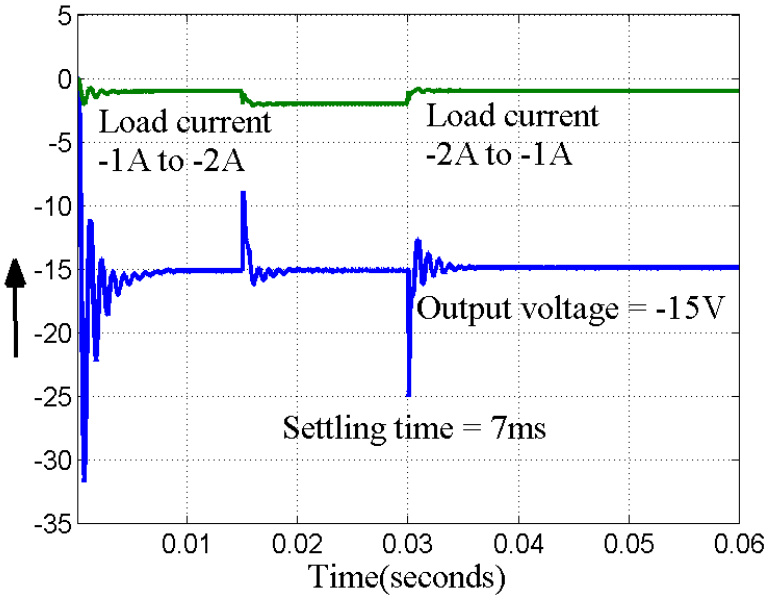


Fig. 3.14: Load transient of CCC for -15V,-2A output

3.8 Closed Loop Operation of CCC at an Output Voltage of -40V

3.8.1 Voltage

The CCC is simulated in boost mode to get an output voltage of -40V with a current of -2A. The output and input voltage are shown in Fig.3.15. It gives an output voltage of V_o = -40V with V_g =20V at the input end. The settling time of the converter is almost 30ms.

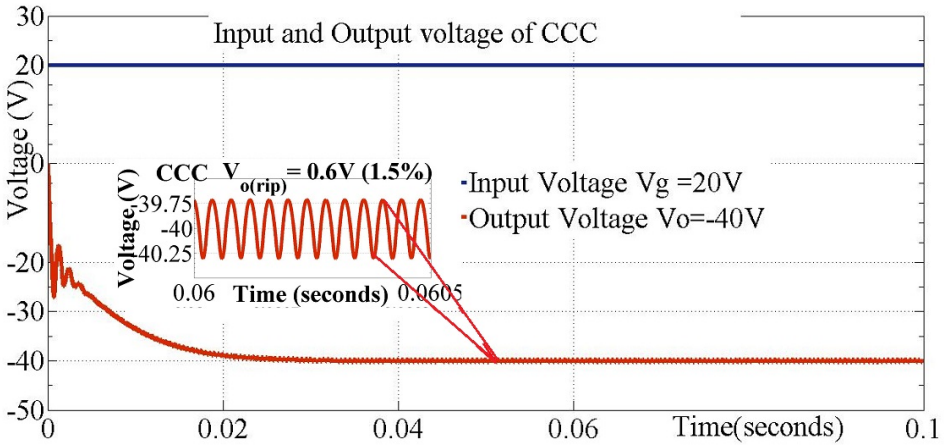


Fig. 3.15: Input and output voltage of CCC. Input voltage = 20V, Output Voltage V_o =-40V, at a load of -2A, Ripple on V_o = 0.6V (1.5% of 40V).

A portion of the output voltage is magnified and is shown in side the Fig. 3.15 as inset. The ripple content on output voltage after the output stabilizes shows that the ripple has a magnitude of 0.6V, which is nearly 1.5% of 40V.

3.8.2 Current

The input and output currents waveforms are shown in Fig.3.16. The observation brings out that the CCC draws, on the average, an input current (shown in Blue) is 4.3A for delivering an average value of output current (shown in Red) is -2A at the output. The input and

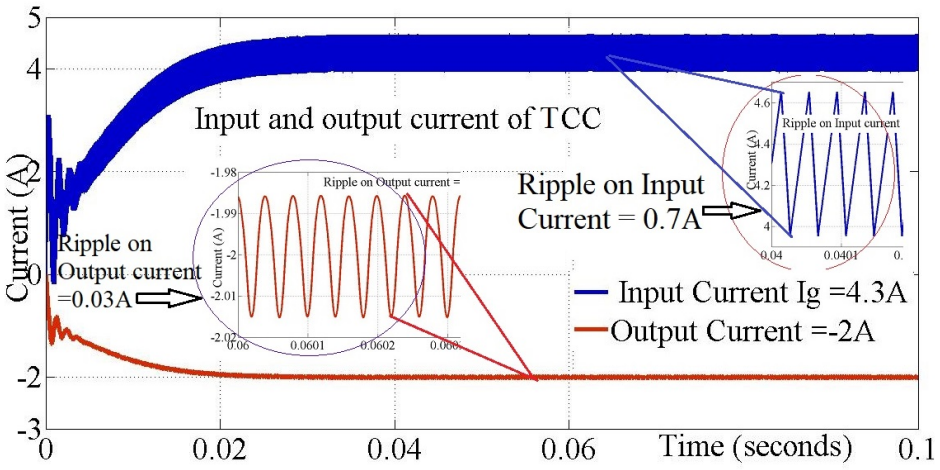


Fig. 3.16: The input and output current waveform of CCC $I_g = 4.3A \& I_o = -2A$ for an output of -40V,-2A.

output currents are zoomed to observe the ripple content. As seen from Fig. 3.16, the ripple (shown in Blue) on input current is 0.7A which is 16.3%. The ripple (shown in blue) on output current is also shown in Fig. 3.16.The output current has a ripple of 0.03A which is 1.5%. With a resistance of 20 ohm the required current is -40/20 = -2A. As seen from Fig. 3.16., the actual load current generated from simulation is -2A.

The switch current shown in Fig. 3.17 brings out that the peak value of switch current for -40V, -2A output is 13.35A, which is 6.7 times

of output current. It is clear from Fig. 3.17 that the duty ratio is

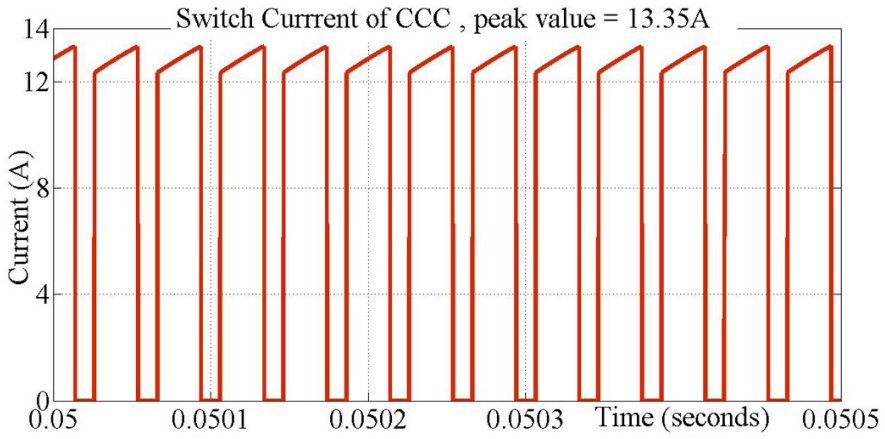


Fig. 3.17: Switch current of CCC for an output of -40V,-2A.

very well beyond 0.5, which is required to obtain the boosted output of -40 V. The duty ratio evaluated from the output Eqn. 3.7 is 0.67. The pulse width for ON time of the switch is 27uS of the total period 40 uS. But the stress of the switching device S_1 due to the high peak current and the duty ratio beyond 0.5 makes the design not suitable for boost operation. However, it is interesting to note that the CCC is possible to produce -15 V from 20 V at a lower duty ratio of 0.43.

3.8.3 Transients

The perfomance of the type III compensator in closed loop is evaluated by conducting line and load transient tests. An additional circuitry along with source voltage inserted in CCC to obtain line trasient response. The line transient for the variation of input voltage input voltage from 17V to 23V at 70 μs is shown in Fig. 3.18

by keeping the load current constant. The reference value of output

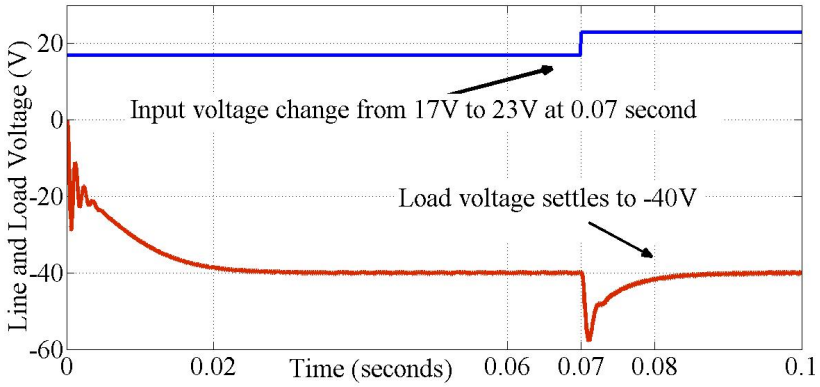


Fig. 3.18: Line transient of CCC for -40V,-2A output

voltage is set to -40V for compensator and operations of CCC. It has found from the line transient response observation that the output settles back to -40V with a settling time of 15ms. The output has a small overshoot and it can be decreased by increasing filter capacitor values, but it may increase settling time hence designed capacitor value is used.

The load transient waveform for the change of load current while keeping the input voltage constant is shown in Fig.3.19. The load resistance is changed by inserting a switching circuit in series with resistive loads. The output voltage settles to the reference value set in the converter in response of load transient by the control of compensator. The load resistor is changed in such a way as to change the load current from -1A to -2A at 30ms. The response shows that the output voltage settles to V_o to -40V, at $I_o = -2A$ after a dip.

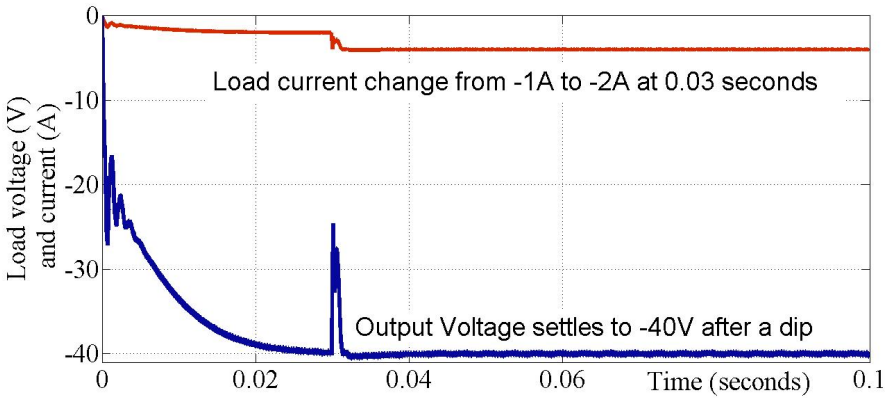


Fig. 3.19: Load transient of CCC at an output of -40V,-2A

3.9 Summary

In the present chapter, the design of conventional cuk converter CCC is discussed in detail and the design is simulated in MATLAB environment in closed loop using compensator realized in z-domain. Both the buck and boost operations have been demonstrated in simulation. The output voltage, switch current, source current along with ripple content both at input and output are plotted. The plot of the switch current reveals that the CCC is possible to produce -15 V from 20 V at a lower duty ratio of 0.43. Both the buck and boost operations have been demonstrated in simulation. However, for the boost operation, that the duty ratio is very well beyond 0.5. Accordingly, the stress of the switching device S_1 due to the high peak current and the duty ratio beyond 0.5 makes the design not suitable for boost operation. The practical realisation of the simulation is given in the following chapter.

Chapter 4

Hardware Realization of Conventional Cuk Converter

4.1 Introduction

The practical realization of the CCC to validate the simulation results is discussed in this section. The complete design of the system including selection of inductors, capacitors circuit, switches and diodes, followed by the realization of the complete hardware on a PCB has been achieved. A resistive load is used for ascertaining the parameters like output voltage, load current, voltage and current transients. Analog ammeters, voltmeters, digital multimeter, digital storage oscilloscope, power quality analyzer are used for measurement of various parameters as above. Though both open and closed loop hardware realizations have been carried out, only closed loop experimental results are shown discussed here.

4.2 Selection of Components

The energy storage components designed for the realization of the CCC for 80W output are tabulated in Table 4.1. While standard

Table 4.1: Design values for the CCC for 80W output

parameter	Values	parameter	Values
V_g	20 V	V_o	-40 V
L_{1a}	0.75mH	L_{1b}	1.5mH
C_1	22μF	C_{o1}	10μF
R_L	20 Ω	f_s	25 kHz

values of capacitors are taken, the inductor is realized by winding the SWG copper wire on E-55 core to get required value of inductance as per design. The number of turns are calculated [81] for $L_{1a} = 0.75mH$ and $L_{1b} = 1.5mH$ as explained below. The ferrite core E-55 selected for winding the copper SWG wire, the area product of the core is given by the general Eqn. 4.1.

$$A_c A_w = \frac{L I_p I_{rms}}{K_w B_m J} \tag{4.1}$$

where A_c - Area of core (m^2), A_w - Area of window(m^2).
L - Inductance in (H), I_p -Peak current (A),
I_{rms} -RMS current (A), J - Current density (A/m^2), B_m - Maximum flux density (T), The number of turns N is given by the Eqn 4.3 for an inductor with inductance L_{1a}, length l_g, permeabilities μ_o, μ_r and area of core A

$$N = \sqrt{\frac{L_{1a} * l_g}{\mu_o * \mu_r * A}} \tag{4.2}$$

Table 4.2: Design values for an inductor

Parameter	Value	Parameter	Value
L_{1a}	0.75 mH	l_g	1 mm
I_p	5 A	I_{rms}	3.54 A
K_w	1 mm	B_m	0.3 T
J	3 A/m^2	μ_o	4 $\pi * 10^{-7}$ H/m
μ_r	1	A	353* $10^{-6}m^2$

The area of the wire $a_c = 3.54/3 = 1.18m^2$, The conductor selected as 0.397 mm^2, SWG = 22, carries 1.5A, So three conductors wound in parallel. The area A = 353 * $10^{-6}m^2$ from E-55 core datasheet.

$$N = \sqrt{\frac{0.75 * 10^{-3} * 1 * 10^{-3}}{4\pi * 10^{-7} * 353 * 10^{-6}}} = 42Turns \tag{4.3}$$

For the inductor L_{1b} =1.5mH the number of turns is given by equation(4.4). $I_p = 2.5$A, $I_{rms} = 2.5/\sqrt{2} = 1.8$ A, $K_w = 1$mm, $B_m = 0.3$ T, Current density J = 3 A/m^2, area of the wire $a_c = 1.8/3 = 0.6m^2$, SWG 20 wire is used.

$$N = \sqrt{\frac{1.5 * 10^{-3} * 1 * 10^{-3}}{4\pi * 10^{-7} * 353 * 10^{-6}}} = 58Turns \tag{4.4}$$

Forty two turns of three wire 22 SWG conductors in parallel are wound on E-55 core and 0.75mH is obtained. Fifty eght turns of single wire 20 SWG conductor is wound on E-55 core and 1.5mH is obtained.

4.3 Practical Implementation of CCC in Closed Loop

The practical realization of CCC has been achieved on electronic circuit board in open loop and closed loop. The converter is realized

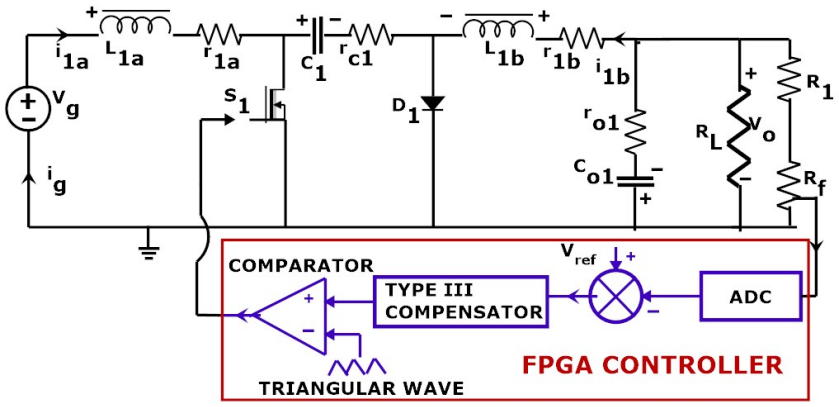


Fig. 4.1: Block diagram for closed loop control of CCC

with an input voltage of 20V and output voltage of -15V and -40V at 2A. In order to implement the feed back, the output voltage is scaled down and applied to 8 bit ADC of ALTIUM FPGA Spartan-3AN Nano controller board. The sensed output is compared with reference voltage and error generated is given to compensator implemented XILINX. For realization, (Fig. 4.1) the compensator along with triangular generator is modelled using XILINX tool of MATLAB. The model is executed on the ALTIUM FPGA controller. The DC output of the type III compensator is compared in the comparator with the bipolar triangular waveform and the PWM output is generated. The obtained PWM pulse sequence is level shifted to boost the voltage and applied to the gate of MOSFET IRF540, to regulate the switching operation.

The circuit diagram of the CCC realized on electronic circuit board is shown in Fig. 4.2. The inductors (L_{1a} and L_{1b}) are wound on E55 ferrite cores, IRF540 MOSFET is used as switch and MUR420 high frequency diode is used to complete the circuit realization. The inductors L_{1a} and L_{1b} are connected respectively to the terminals L1

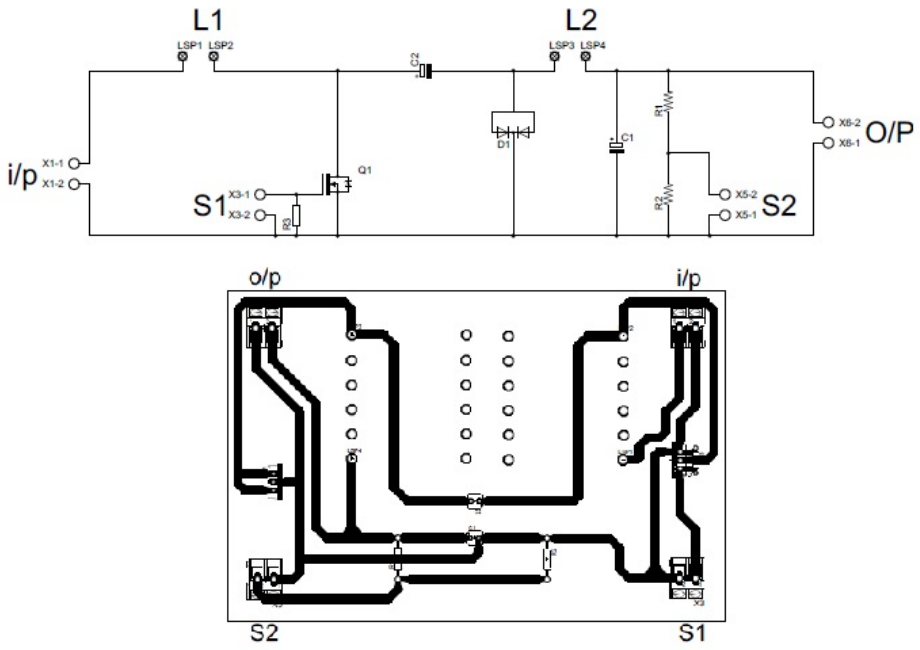


Fig. 4.2: Practical circuit diagram of CCC and its layout

and L2 of Fig. 4.2. The voltages and currents are measured respectively at the points i/p, o/p and S1, S2. The complete block schematic of the realization is given in Fig. 4.1.

For testing the CCC, the input voltage is applied from a 30V, 5A, DC Power supply, and at the output, a resistive load of 100 ohm rheostat is used. The output voltage is divided by using a potential divider circuit of 1:11 and is terminated at S_2. The current sensors of LA55P are used for measurement input and output currents. The current sensor is scaled as 1V = 1A to measure the current in oscilloscope. The output voltage, input voltage, output current, input current are measured using TEKTRONIX 50 / 100MHz Digital Storage Oscilloscope (DSO).

4.4 Measurements from Hardware Realized at an Output -15V, - 2A

The photograph depicting the hardware realization of CCC is given in Fig. 4.3. The CCC realized along with all ancillary power supplies and monitoring devices and instruments are marked clearly in the photograph.

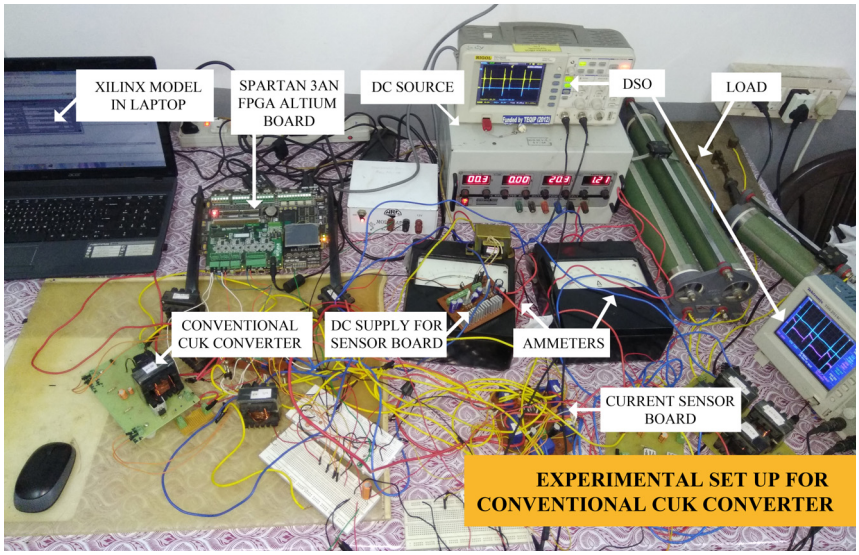


Fig. 4.3: Photogaph: Experimental set up for CCC along with XILINX FPGA controller board

4.4.1 Voltage

The CCC is tested by applying an input voltage of 20V (from a 30V, 5A power supply). The steady state output voltage measured on the

oscilloscope is shown in Fig. 4.9 as -15V (in red) at output load current of -2A. The input voltage of 20 V is shown in blue in Fig. 4.9.

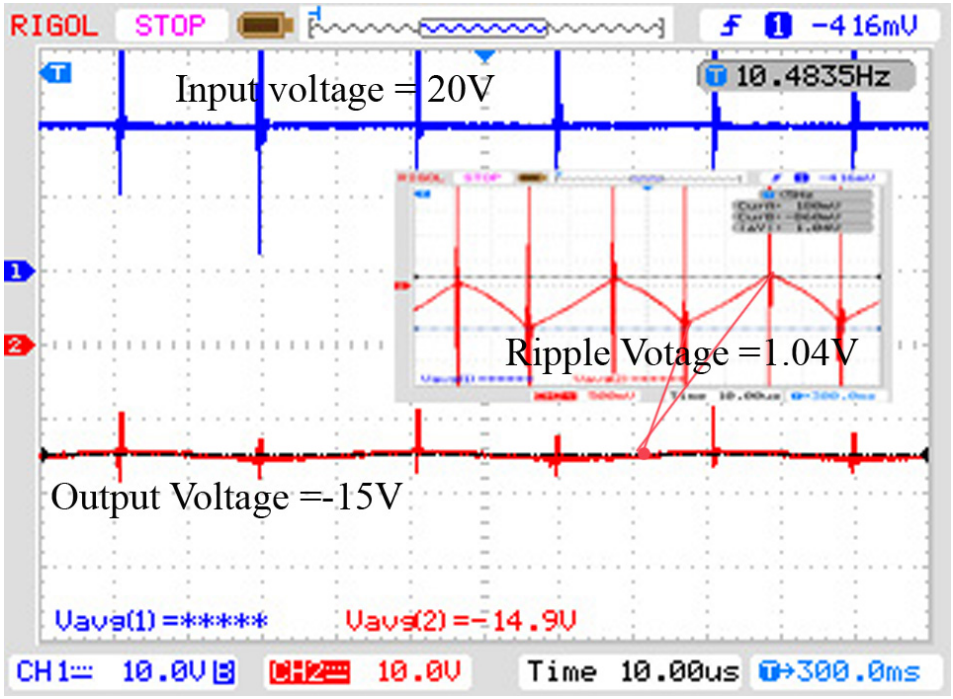


Fig. 4.4: For the input voltage of 20V (shown as blue), the steady state output voltage is measured as -15V (in red) at -2A output load current, Ripple content on output voltage of CCC (shown as red in inset) at -15V is 1.04V

However, on a finer measurement scale, it is seen that that the output voltage has a certain amount of ripple. As shown in Fig. 4.9. the ripple on output voltage of -15V, at a load current 2A is measured as 1.04, which works out to be 7%.

4.4.2 Current

The waveform of the input and output current are shown in Fig. 4.5. With a resistive load of 7.5 Ω connected across -15V output, the

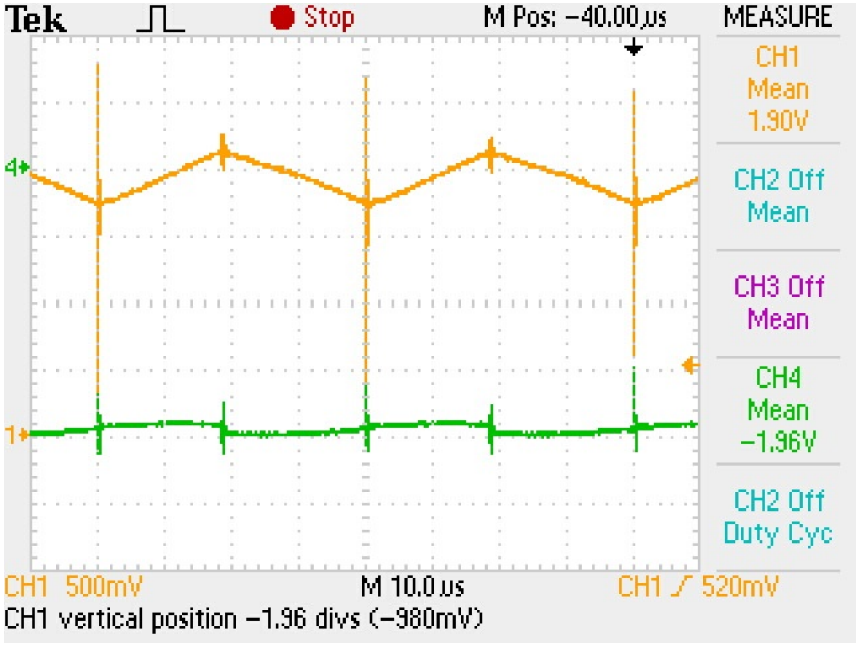


Fig. 4.5: Ripple currents at Input (in amber) and output (in green) of the CCC. The input ripple is 500 mA (26%), while the output ripple is -100 mA (5%).

converter produces an output current of -2A, when it draws an input current of 1.9A. Current sensors are used to measure input and output currents. The current sensor is scaled to measure 1A as 1V on the Oscilloscope . The ripple on the output current shown in Fig. 4.5 measures as 100mA (in green), which is 5% (0.1/2) at the measured output current of -2A. The ripple for the corresponding

input current of 1.9 A is 400mA (in amber), which is 26% (0.5/1.9) of the measured current. It is interesting to note that the amount of spike at the output substantially less that the input. This could be attributed to insufficient grounding and isolation of the current probe used.

Switch current of CCC, primarily responsible for energy transfer from input to output, is shown in Fig. 4.6. The peak Switch current of

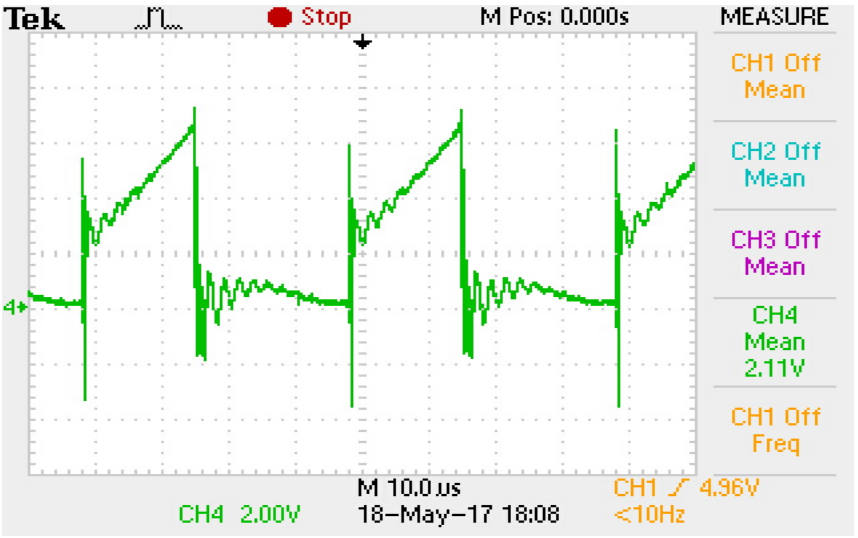


Fig. 4.6: Switch current of CCC at -12V, peak value =6.6A

CCC is observed in DSO is 6.5A at an output of -15V, -2A. The pulse train with a period of 40 μs and a pulse duration of 18 μs switches S1 in Fig. 4.2 and 4.1. The spikes appearing in all the voltage and current waveform at output can be attributed to this period of 40 μs.

4.4.3 Transients

The response of the CCC to input line transient is measured by changing input voltage (in amber) from 15 to 25V to assess the response. It can be seen that the output (in green) settles to -15V, with a settling time of 50ms as shown in Fig. 4.7. The line voltage is

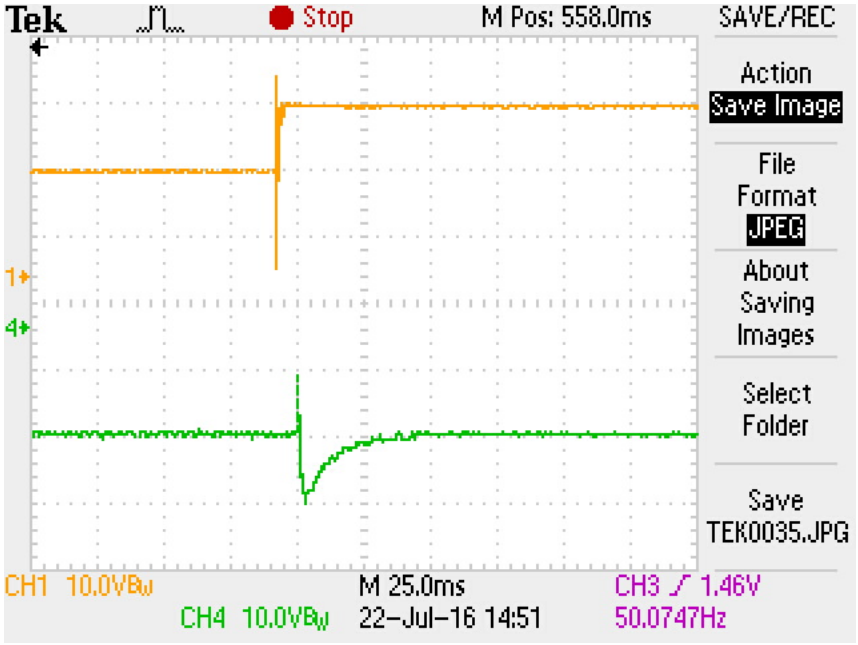


Fig. 4.7: Line transient (voltage) of the CCC at -15V output. The input voltage variation is shown in amber, while the output is in green

measured by using a manual switching arrangement to change the input voltage between two set values of 15V and 25V. There is an under shoot of -25V at the output, in response the sudden change of 25 V input; but the settling time very well within acceptable limits.

The transient behavior as seen from the load side is shown in Fig. 4.8. From Fig. 4.7, it is clear that there is an undershoot of output

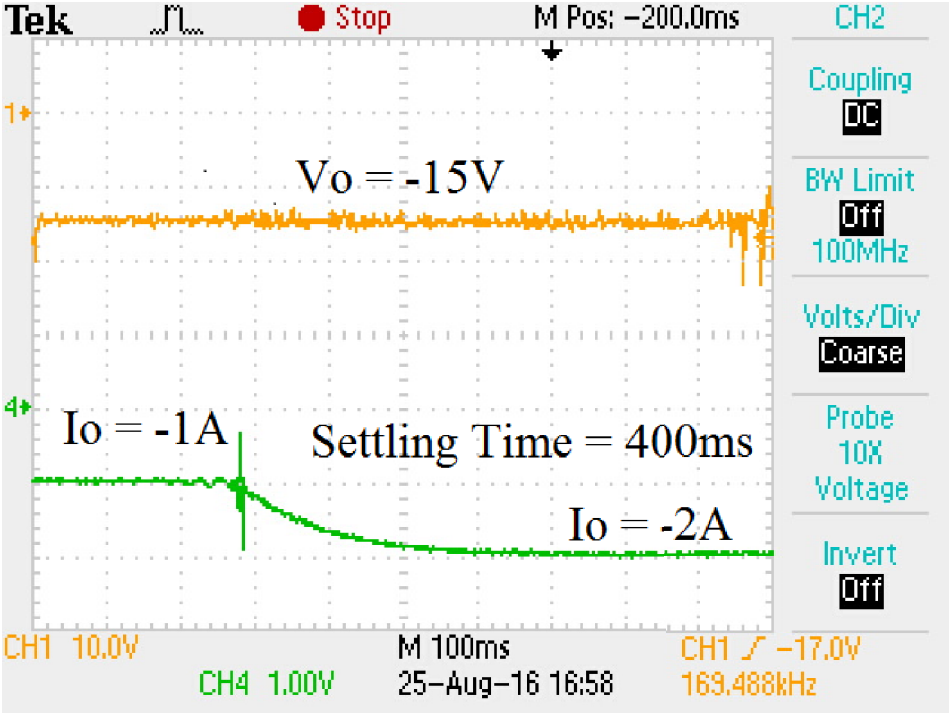


Fig. 4.8: Load transient (current) of the CCC at -15V output. The load current variation is shown in Green, while the output in Amber settles to -15V

voltage because of step change. Following this change in voltage, the load current has a change from -1A to -2A and load voltage also settles back to -15V, with a settling time of about 400ms. A manual switching arrangement is made by connecting two rheostats in series to change the current into two set values of -1A and -2A. The choice of the capacitor C_{o1} of Fig. 4.1 decides the settling time.

4.5 Practical Realization of CCC at -40V, - 2A Output

The experimental implementation of CCC for buck operation is detailed in section 4.4. The CCC is practically validated also for the boost operation to provide an output of -40V, -2A.

4.5.1 Voltage

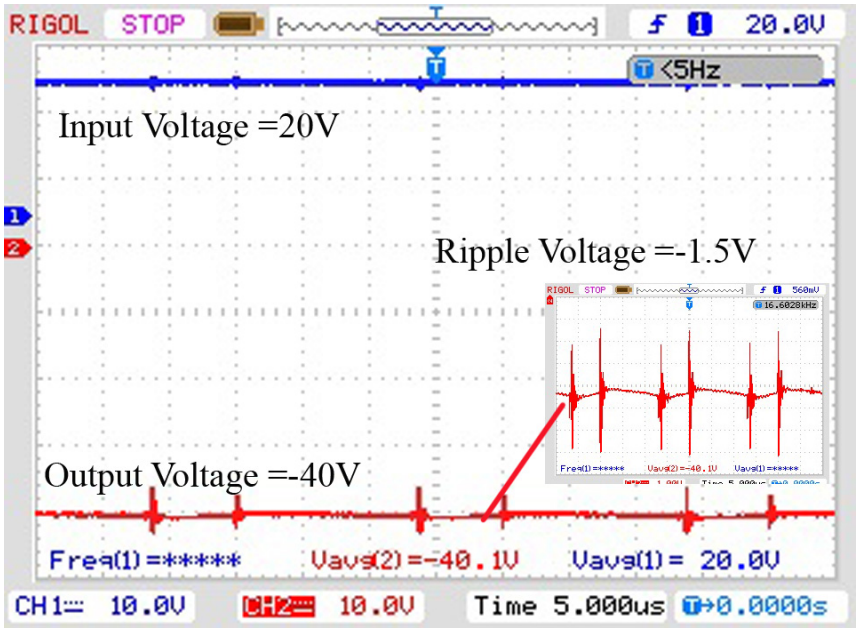


Fig. 4.9: For the input voltage of 20V (shown as blue), the steady state output voltage is measured as -40V (in red) at -2A output load current, ripple content on output voltage of CCC (shown as red in inset) at -40V is 1.5V

The CCC is tested by applying an input voltage of 20V (from a 30V, 5A power supply) also to measure a steady state output of -40V ,-2A. The input voltage of 20 V is shown in blue in Fig. 4.9. However, on a finer measurement scale, it is seen that that the output voltage has a certain amount of ripple as shown in Fig. 4.9. The ripple on output voltage of -40V, at a load current- 2A is measured as 500 mV, which works out to be 1.25%.

4.5.2 Current

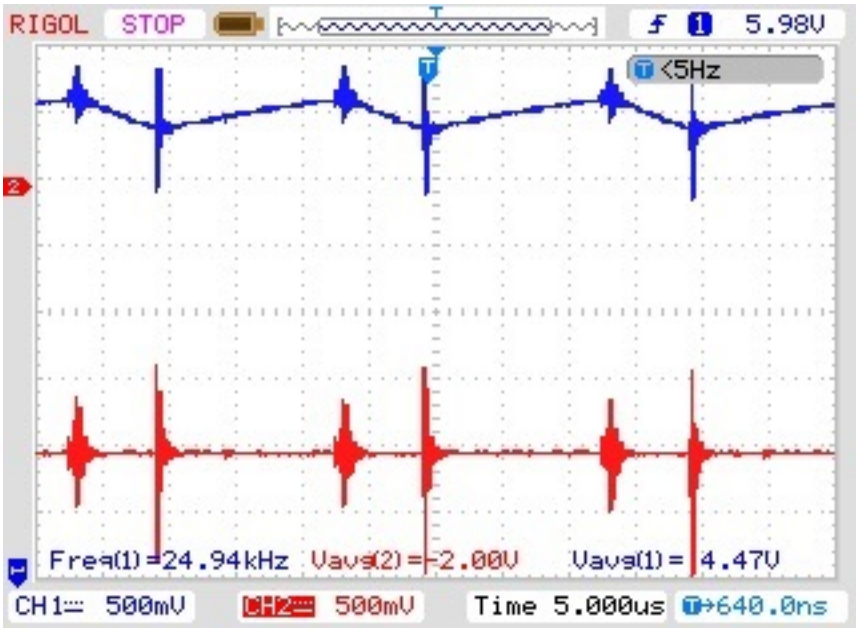


Fig. 4.10: Input and Output current : (current scale, 1V=1A) Source current I_g (in blue) = 4.47A, Ripple on input current =500mA (11.2%) ; Output current I_o(in red) =-2A, the output ripple is -100 mA (5%).

The waveform of the input and output current are shown in Fig. 4.10. With a resistive load of 7.5 Ω connected across -40V output, the converter produces an output current of -2A, when it draws an input current of 4.47A.

The current sensor is scaled to measure 1A as 1V on the Oscilloscope. The ripple on the output current shown in Fig. 4.10 measures as 100mA (in Red), which is 5% (0.1/2) at the measured output current of -2A. The ripple for the corresponding input current of 4.47 A is 500mA (in blue), which is 11.2% (0.5/4.47) of the measured current. It is interesting to note that the amount of spike at the output substantially less that the input. This could be attributed to insufficient grounding and isolation of the current probes used.

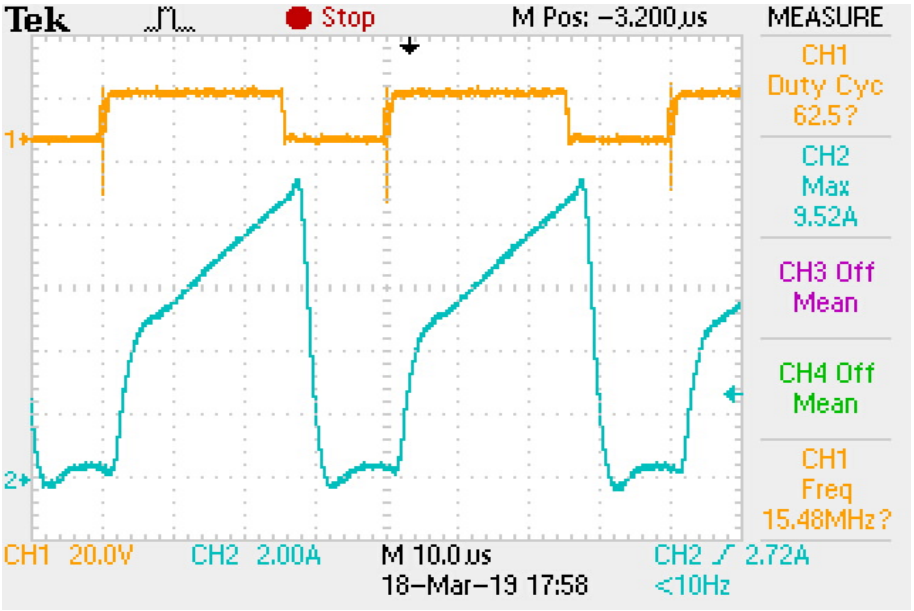


Fig. 4.11: Switch current of CCC at -40V,-2.11A, peak value =9.52A, d = 0.63

The switch current of CCC, primarily responsible for energy transfer from input to output, is shown in Fig. 4.6. The peak switch current of CCC is 9.52 at -40V, -2.11A which is 4.5 times the load current. The pulse train with a period of 40 μs and a pulse duration of 25 μs switches S1 in Fig. 4.1 and 4.2. The spikes appearing in all the voltage and current waveform at output can be attributed to this period of 40μs.

4.5.3 Efficiency

The measurement values of input and output parameters are tabulated in Table 4.3 to plot the efficiency curve.

Table 4.3: Efficiency of CCC converter at $f_s = 25kHz$,d=0.43

V_g (V)	I_g (A)	V_o (V)	I_o (A)	Efficiency (%)
20	0.405	-12	-0.595	88
20.2	0.7	-12.1	-1.05	89.9
20.3	0.9	-12	-1.4	90.2
20.2	1.3	-12	-1.97	90.02
20.2	1.54	-12	-2.35	90.7
19.9	1.92	-12	-2.89	90.7
19.8	2.47	-11.8	-3.52	84.9

The converter is tested with an input of 20V and the output is controlled to -12V. The rheostat load is varied in wide range for a load current from 0.5A to 3.5A and the input current is noted. Also the variation of output voltage is measured to complete the evaluation. The efficiency is calculated and the converter provides a tight regulation of output voltage for the variation of load current

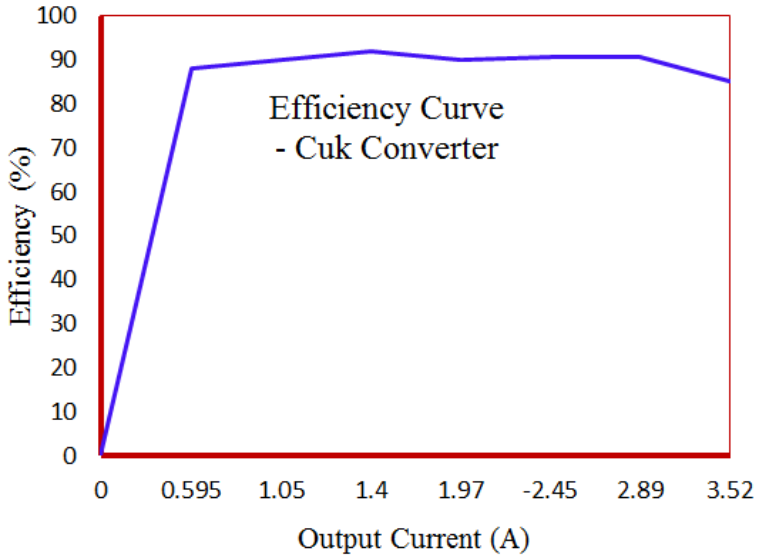


Fig. 4.12: Efficiency of cuk converter at -12V, -2A

from 0.5A to 3.5A. The efficiency curve of CCC is plotted in Fig.4.12, the average efficiency is 89%

4.6 Summary

Conventional Cuk Converter is designed, simulated and experimentally validated in closed loop at -15V and -40V at -2A output. From the observations and characteristics it can be concluded that ripple content on the source side current is high about 25% for an output voltage of -15V. Also the peak current of the switch is low when the converter operates with duty ratio lessthan 0.5. But to provide an output voltage of -40V, the converter has to operate with a duty ratio of 0.67 (above 0.5). The peak

Table 4.4: Results for CCC at $f_s = 25kHz$,d=0.43

parameter	Simulation Resutls	Experimental Results
V_g	20v	20v
V_o	-15v	-15v
I_g	1.8A	1.9A
I_o	-2A	-2A
I_{grip}	0.45A (27%)	500mA (26%)
I_{orip}	0.024A (1.2%)	100mA (5%)
V_{orip}	0.18V (1.2%)	1.04V (7%)
$I_{sw_{pk}}$ at -40V	13.35A	9.52A
$I_{sw_{pk}}$, at -15V	4.1A	6.5A
Line Transient at -15V	30ms	50ms
Load Transient at -40V	15ms	400ms
Average Efficiency	–	89%

current of the switch for -40V, -2A output is high. The findings from the systematically built hardware from this chapter is published as a paper, that substantiates credence to the work executed. The proposed methods to reduce current ripple and switching stress are discussed in next chapter

Chapter 5

Proposed Interleaved Cuk Converter

5.1 Introduction

The practical realization and the evaluation of the performance of the CCC was presented in the last chapter. The CCC was shown to operate both in the buck and the boost modes of operation. While operating the CCC on the boost mode,the inductor present on input side of the CCC was seen to be helping to reduce the ripple on source current, as was illustrated in Fig. 3.16 and 4.10. But the amount of ripple on DC source current in high and it can inject harmonics to parent AC source. It was also seen that the switching device gets heavily stressed since the duty ratio to obtain boost operation is high.

With a view to reduce the above limitations in the operation of DC to DC converter, an interleaved coupled boost converter is analysed

in [9], which gives better result than boost converter by reducing ripple on input side. The current stress on the switch is distributed in interleaved converter circuit, thereby reducing the switching losses to a great extent. Obviously, the current sharing feature of interleaved converter reduces the ripple on input current. It is also a known fact that the interleaved converter produces output voltage less than input voltage, when duty ratio is less than 50%. In order to

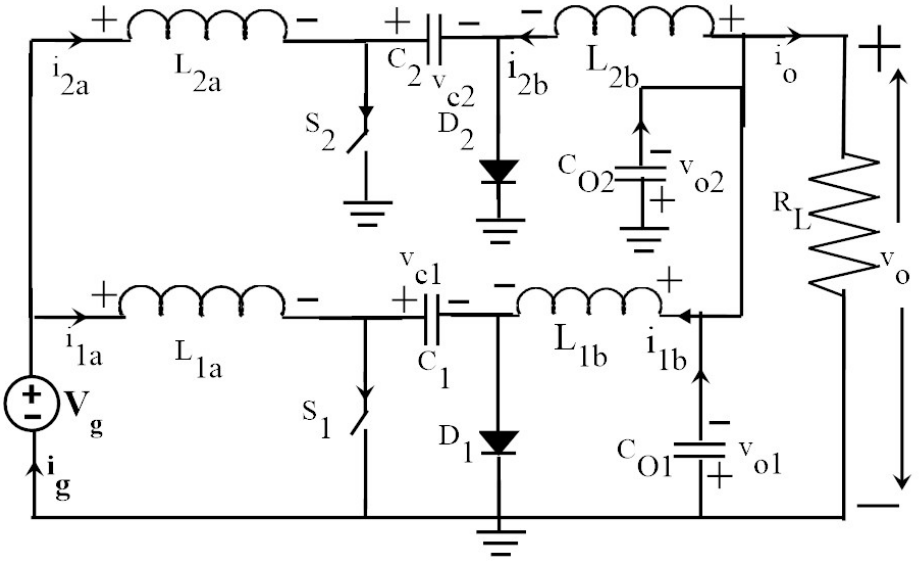


Fig. 5.1: Basic circuit diagram of Proposed ICC

alleviate the above mentioned issues an Interleaved Cuk Converter (ICC) using Phase Shifted Pulse Width Modulation scheme (PSPWM) is proposed in the present work. Fig. 5.1 illustrates the circuit of the Proposed ICC. The PSPWM scheme is illustrated in Fig. 5.2, (to be read in the context of Fig. 5.1). The basic idea of PSPWM is to divide the total gating pulse T_{ON} by 2 and generate two pulses for S_1 ON and S_2 ON, to switch each leg of the

interleaved configuration. The delay between S_1 ON and S_2 ON is carefully chosen to ensure low harmonic injection to the parent AC source.

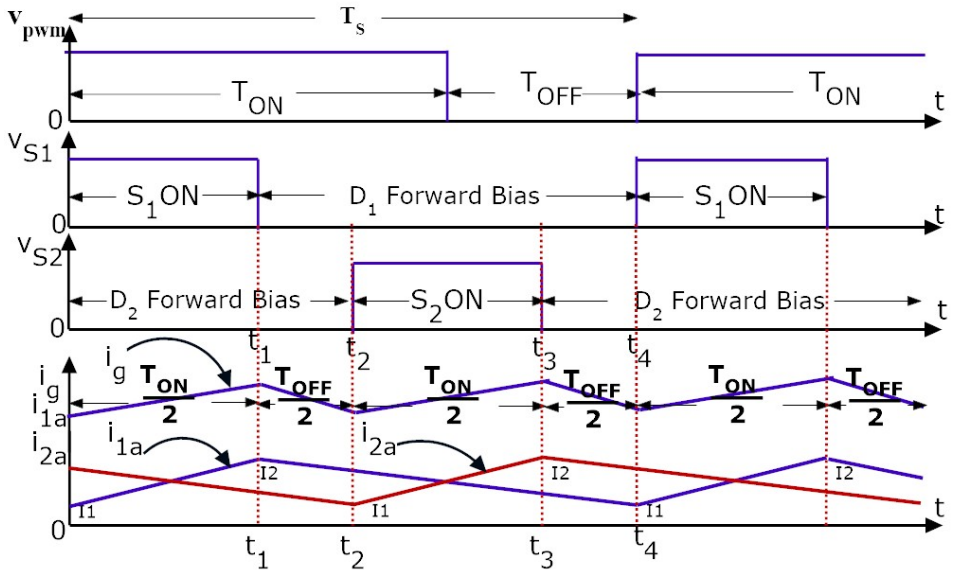


Fig. 5.2: Waveforms of PSPWM technique: V_{PWM} = gate voltage of switch of CCC; V_{S1} and V_{S2} gate voltages of the two legs of Proposed ICC; i_{1a} and i_{2a} : current through inductors L_{1a} and L_{2a}; i_g: source current of Proposed ICC.

The Proposed ICC topology is derived and developed for practical realization. The converter consists of four inductors, four capacitors, two switches and two diodes (Fig. 5.1). A modified PWM [9] as shown in Fig.5.2, produces a switching waveform V_{S2}, which is applied to second switch S_2, in place of the of the conventional inverted PWM pulse sequence. For this, a phase shifted PWM technique is developed and used to trigger the switches. The output voltage is scaled and

fedback through a transfer function, whose output is compared with reference value. The error processed in compensator, generates the DC signal from the controller, which is compared with triangular waveform to generate the PWM signal. From the PWM signal generated, the ON time of the PWM signal is further divided into two. The first pulse is applied to the switch S_1 (Fig. 5.1) during the beginning of first half cycle of switching frequency and the second pulse is applied to the switch S_2, during the beginning of second half cycle of the switching frequency. During the OFF time of pulses the diodes will be active with respect to the switches.

Referring to Fig. 5.1 and 5.2 when the switch S_1 is ON, the inductor L_{1a} is connected to the source, it will be magnetised and capacitor will be discharged, as in the case of the CCC. When the switch S_1 is OFF, the current will flow through diode D_1 and inductor L_{1a} transfers stored energy to the load. This will happen during first half of the switching cycle. So the power transfer from source to output takes place on every half of the period. In Sec. 5.2 below the converter analysis done using state space averaging method.

5.2 Modelling of Proposed ICC

5.2.1 Mode 1 - S_1 ON and S_2 OFF (0 to t_1)

During the period $t_1 = d_1T$, where $d_1 = \mathrm{d}$ is the duty ratio ($0 < \mathrm{d} < 0.5$) of switch S_1, the switch S_1 turned ON, inductor current i_{1a} rises from initial value I_1 and reaches to peak value I_2. With the switches S_1 in ON and S_2 in OFF state, the equivalent circuit diagram of Fig. 5.1 is shown in the Fig.5.3, where L_{1a} charges up and at the same time inductor L_{2a} discharges (refer the timing diagram in Fig.5.2). During

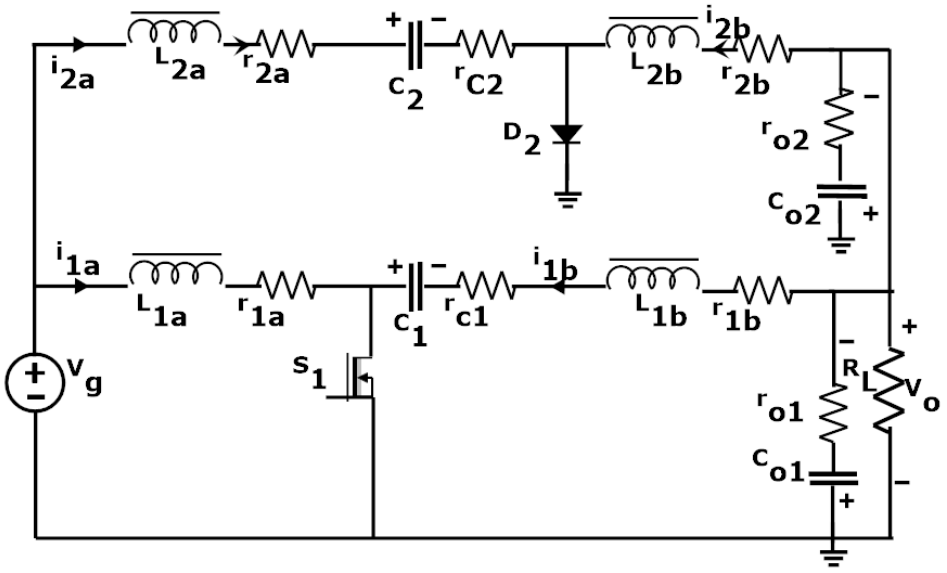


Fig. 5.3: ICC diagram of Fig. 5.1, when S_1 is ON and S_2 is OFF

this time, the capacitor C_{o1} also discharges, charging the inductor L_{1b}. The stored energy in L_{2b} transfers to C_{o2}. Also the capacitor C_1 discharges through C_1, S_1, C_{o1}, L_{1b} and R_L, hence transfers stored energy in the capacitor to the load to produce output voltage. At t_1, the switch S_1 opens and inductor L_{1a} starts discharging. i_g, the source current in the Fig. 5.2 shows the sum of the currents i_{1a} and i_{2A} from the source. The state equations [82] required to complete the modeling for switches S_1 ON & S_2 OFF are derived in Appendix B.1

The load current is assumed to be constant, ripple current equation [4] for ideal ICC is derived as shown in Eqn. (5.1), (5.2) and (5.3). It is assumed that $L_{1a} = L_{2a}$, V_g is the voltage of the DC source current.

$$\Delta I_{L1a} = \frac{(t_1 - 0)V_g}{L_{1a}} \tag{5.1}$$

$$\Delta I_{L2a} = \frac{(t_1 - 0)(V_g - V_{c2})}{L_{2a}} \tag{5.2}$$

The ripple content on source current is given by equation (5.3)

$$\Delta I_{r_{mode1}} = \frac{t_1 V_{c2}}{L_{2a}} \tag{5.3}$$

5.2.2 Mode 2 - S_1 OFF and S_2 OFF (t_1 to t_2)

When both switches S_1 OFF and S_2 are OFF, with the circuit of Fig. 5.1 as shown in Fig.5.4, both inductors L_{1a} and L_{2a} are discharging and stored energy transfers to capacitors C_1 and C_2 respectively. At the same time inductors L_{1b} and L_{2b} are discharging as shown in Fig.5.2, transferring their energy to load. During this mode all inductors are discharging and capacitors C_1, C_2, C_{o1} and C_{o2} are charging up. Assuming that the inductor current is linear, and the diodes D_1 and D_2 are identical, the ripple content on DC source current for ideal ICC is derived by Eqn. (5.4), (5.5) and (5.6), below.

$$\Delta I_{L1a} = (t_2 - t_1)(V_{c1} - V_g)/L_{1a} \tag{5.4}$$

$$\Delta I_{L2a} = (t_2 - t_1)(V_{c2} - V_g)/L_{2a} \tag{5.5}$$

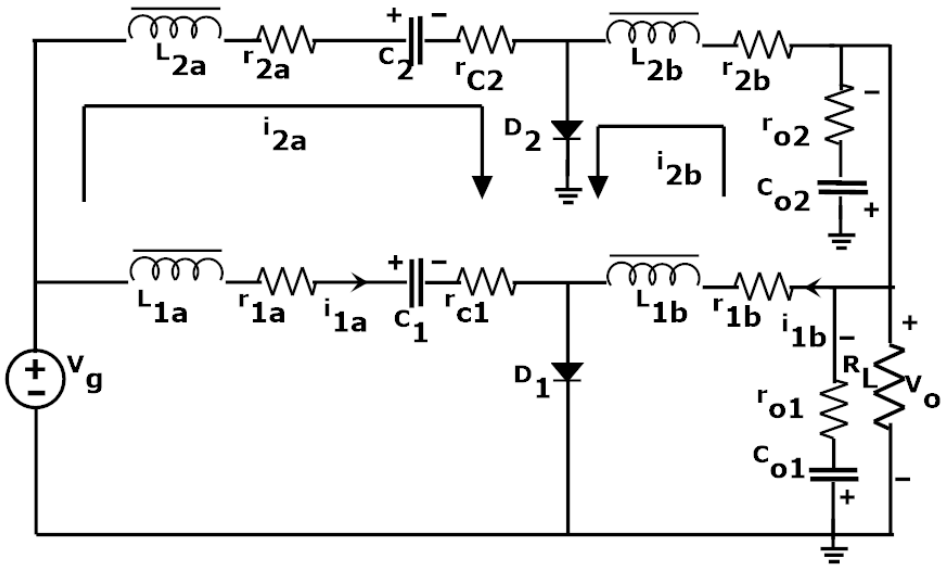


Fig. 5.4: Proposed ICC circuit diagram when both switches S_1 and S_2 are in OFF state

The ripple on source current is zero as per equation (5.6)

$$\Delta I_{r_{mode2}} = (t_2 - t_1)(V_{c1} - V_{c2})/L_{2a} = 0 \tag{5.6}$$

where $V_{c1} = V_{c2}$, assume equal values for capacitors.

The state space equations required to complete modelling [82] for Mode-2 is shown in appendix B.2.

5.2.3 Mode - 3: S_1 OFF and S_2 ON (t_2 to t_3)

In this mode the switch S_1 is kept OFF and S_2 turned ON leaving the circuit of Fig. 5.1, as shown in Fig.5.5. The inductor L_{2a} charges

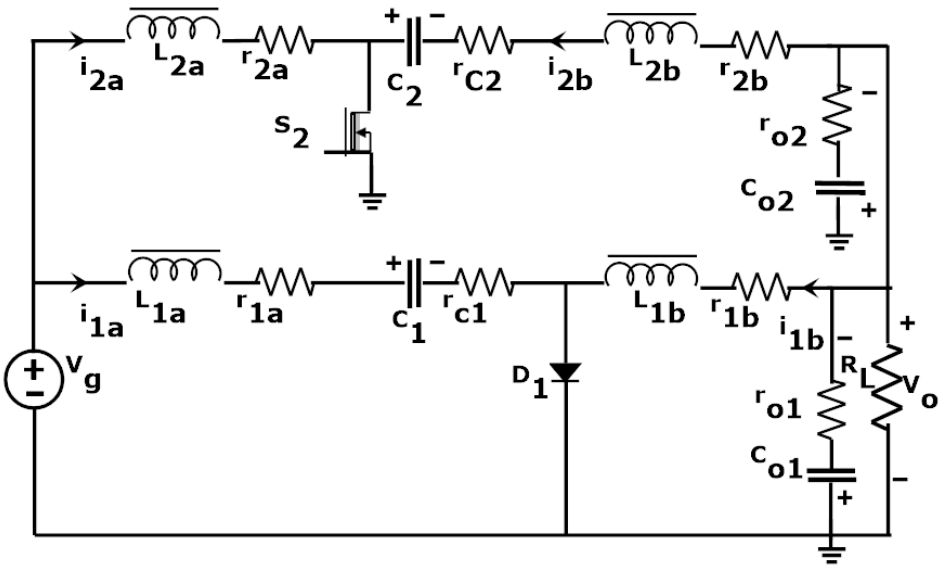


Fig. 5.5: ICC circuit diagram when switches S_1 in OFF and S_2 in ON states

and at the same time inductor L_{1a} discharges (Fig.5.2). The stored energy in L_{1a} transfers to C_1. At this time, the capacitor C_2 discharges through S_2, as indicated by i_{2b} in Fig.5.5, with C_2, C_{o2}, L_{2b} and R_L in circuit. As a result stored energy in the capacitor C_2 appears as voltage across the load. As in the case of Fig.5.3, where i_{1b} was responsible for producing the output voltage, i_{2b} produces the voltage across the load in this case. Equations for ripple on source current are as given below by Eqn. (5.7), (5.8) and (5.9).

$$\Delta I_{L1a} = \frac{(t_3 - t_2)(V_g - V_{c1})}{L_{1a}} \tag{5.7}$$

$$\Delta I_{L2a} = \frac{(t_3 - t_2)V_g}{L_{2a}} \tag{5.8}$$

$$\Delta I_{r_{mode3}} = \frac{(t_3 - t_2) * (-V_{c1})}{L_{2a}} \tag{5.9}$$

It is obvious that the ripple on source current depends on the voltage across the energy storage capacitor, inductor value and OFF time of the period. The state space equations to complete the modelling can be deduced as shown in Appendix B.3.

5.2.4 Mode 4 - S_1 OFF and S_2 OFF (t_3 to t_4)

When both switches S_1 and S_2 are in OFF, the situation is as shown in Fig.5.4. This mode is in effect a repetition of mode 2. (discussed in section 5.2.2). With this a full cycle is completed.

5.3 Output Equation of Proposed ICC

The output equation of Proposed ICC can be derived as follows. During Mode -1, Capacitor C_1 acts as primary means of storing and transferring energy from the input to the output. Under steady state conditions average inductor voltages V_{La1} and V_{Lb1} over a period are zero. Hence

$$V_{C1} = V_g + V_{o1} \tag{5.10}$$

where V_{C1} and V_{o1} are voltage across capacitors C_1 and C_{o1} respectively. The volt-sec balance of switch S_1 is given by

$$\frac{V_g * d * T_s}{2} + \frac{(V_g - V_{c1}) * (1 - d) * T_s}{2} = 0 \tag{5.11}$$

where T_s is switching period. Substituting equation (5.10) in equation (5.11), the output voltage across C_{o1} is

$$V_{o1} = \frac{V_g d}{(1-d)} \tag{5.12}$$

where $d = \frac{T_{on}}{T_s/2}$ and T_{on} is on time of switch S_1. Considering the polarities of diodes the output current is in the negative direction along with output voltage with respect to input and thus the converter works in quadrant III of input-output. Hence for the Proposed ICC both step up and step down for output voltage takes place as per Eqn. (5.12). Also ripple cancellation takes place as confirmed by equations (5.1), (5.5) and (5.6). Since the both the legs of the circuit in Fig. 5.1, are parallel, the output, $V_{o2} = V_{o1}$. The converter works satisfactorily d<0.5. The duty ratio of $d > 0.5$ provides overlap of pulses for turn ON switches, it creates issues on inductor charging and discharging and hence d > 0.5 is not recommended for design.

5.4 Design of Components

In this section, the components L_{1a}, L_{1b}, L_{2a}, L_{2b}, C_1, C_2, C_{o1}, C_{o2}, S_1, S_2, D_1 and D_2 are designed [4] systematically, so as to conduct simulation and hardware verifications of proposed ICC.

5.4.1 Design of Inductor - L_{1a}, L_{2a}, L_{1b} and L_{2b}

From Eqn. (5.1) the inductor value can be designed for an input voltage V_g of 20V and an output voltage V_o of -40V.

1. First of all the duty ratio d is obtained by substituting input and output voltages in the Eqn.(5.12), when -40=$\frac{20 * d}{1 - d}$, which in turn gives d = 0.67.

2. The specified output power is 80W and load current (-2A) are restricted to suit the laboratory set-up, available, when the load resistance is $-80/-4$ =20 Ω. The source current for providing 80W power is 80/20 =4A.

3. Permitting 20% ripple on input current, which is 20*4/100 =0.8A, at a switching frequency f_s as 25 kHz, the inductor value is obtained from Eqn.(5.1) $L_{1a} = \frac{20 * 0.67}{25 * 1000 * 0.2 * 0.4 * 2} = 0.335mH.$

   (Referring to Eqn.(5.1), here Δi_{1a} = [(0.2*4)*2], where the last factor 2 accounts for the interleaved operation).
   L_{1a} should be greater than 0.335mH, in order to ensure continuous conduction, hence it is selected as 0.38mH. L_{2a} is assumed to be same as L_{1a}.

4. $L_{1b} = \frac{20 * 0.67}{25 * 1000 * 0.4 * 2} = 0.67mH.$

   L_{1b} chosen to be greater than 0.67mH, as 0.75mH.
   L_{2b} is assumed to be same as L_{1b}.

5.4.2 Design of Filter Capacitors - C_{o1}, C_{o2}, Energy Storage Capacitors - C_1 and C_2

The capacitor C_{o1} is charged by L_{1b} and designed for 1% ripple on output voltage as

$$C_{o1} = \frac{\Delta i_{1b}}{\Delta V_o * 8 * f_s}$$

With $\Delta i_{1b} = 0.2$ and $\Delta Vo = 0.4$ for V0 = -40 V,

$$C_{o1} = \frac{0.2}{8 * 0.4 * 25000} = 2.5\mu\text{F}$$

C_{o1} is chosen to be greater than 2.5 μF and it is assumed as 10 μF. Also C_{o2} is taken to be same as C_{o1}.

The capacitor C_1 is primarily responsible for energy transfer and is designed using the relationship, $C_1 = \frac{d^2 V_g}{2 * (1-d) * R_L * \Delta V_{c1} * f_s}$

Here $V_{c1} = V_g + V_o = 60$V and $\Delta V_{c1} = 5\%$ of V_{c1} =3V.

$$C_1 = \frac{0.67^2 * 20}{2 * 0.33 * 20 * 3 * 25000} = 9.1\mu\text{F}$$

C_1 is greater than 9.1 μF and it is assumed as 10 μF. Also C_2 is assumed same as C_1

To sum up, the designed values from sections 5.4.1 and 5.4.2 for 80W output from the proposed ICC are tabulated as shown in Table 5.1.

Table 5.1: Design values for the proposed ICC

parameter	Values	parameter	Values
V_g	20V	V_o	-40V
$L_{1a} = L_{2a}$	0.38mH	$L_{1b} = L_{2b}$	0.75mH
$C_1 = C_2$	10 μF	$C_{o1} = C_{o2}$	10 μF
R_L	20 Ω	f_s	25 kHz

5.5 Compensator Design - State Space Averaged Model of Proposed ICC

The output voltage of the Proposed ICC, as per the design given in Sec. 5.3 is stabilized using the feedback and the compensator shown in Fig. 5.8. It can be seen that the scaled output voltage is sensed and compared against the reference value. The error generated is sent though the compensator, designed to ensure the gain and phase margins required for the stabilization. The output DC signal of the compensator is used to modulate the PSPWM to switch the power supplies. Towards this, the derivation of the transfer function of the compensator using the state averaged model is discussed below. Though the approach is similar to what was discussed in Sec. 3.5, considering the changes in the definition of the state vector and the system matrices as a result of the change in topology, the subtle differences in the derivation of the transfer functions are presented below. As in the case of CCC, a type III compensator has been included in the design here also. The detailed derivation of the state space model for each mode of operation is given Appendix B.1. Referring to Fig. 5.3, 5.4 and 5.5, the state variables are taken to be

$$\left[\ x(t)\ \right] = \left[\ i_{1a}(t) \quad i_{1b}(t) \quad i_{2a}(t) \quad i_{2b}(t) \quad v_{c1}(t) \quad v_{c2}(t) \quad v_{o1}(t) \quad v_{o2}(t)\ \right]^{\mathrm{T}}$$

where
$i_{1a}(t)$, $i_{1b}(t)$, $i_{2a}(t)$, $i_{2b}(t)$ are current through respective inductors and $v_{c1}(t)$, $v_{c2}(t)$, $v_{o1}(t)$, $v_{o2}(t)$ are voltage across respective capacitors.

Defining the sate equation as $\dfrac{dx(t)}{dt} = Ax(t) + Bu(t)$
and y(t) = C x(t)+ E u(t)
The small signal ac model of the circuit [77] is given below.
$\dfrac{d\hat{x}(t)}{dt} = A\hat{x}(t) + B\hat{u}(t) + (A_1 - A_2)X\hat{d}_1(t) + (A_3 - A_4)X\hat{d}_2(t) + (B_1 -$

$B_2)U\hat{d_1}(t) + (B_3 - B_4)U\hat{d_2}(t)$
$\hat{y}(t) = C\hat{x}(t) + E\hat{u}(t)$
where the variables $\hat{x}(t)$, $\hat{u}(t)$, $\hat{d}(t)$ and $\hat{y}(t)$ are small ac variations bound to their quiescent steady state values X, U, d and Y respectively.

The A,B, C and E matrices are now defined as shown below, corresponding to the different modes of operation:
$A = A_1 * d_1 + A_2 * d_1' + A_3 * d_2 + A_4 * d_2'$.
$B = B_1 * d_1 + B_2 * d_1' + B_3 * d_2 + B_4 * d_2'$.
$C_{R1} = d_1 * C_{mode1R1} + d_1' * C_{mode2R1} + d_2 * C_{mode3R1} + d_2' * C_{mode4R1}$.
$C_{R2} = d_1 * C_{mode1R2} + d_1' * C_{mode2R2} + d_2 * C_{mode3R2} + d_2' * C_{mode4R2}$
$E = E_1 * d_1 + E_2 * d_1' + E_3 * d_2 + E_4 * d_2'$.

where d_1 and d_2 are duty ratios which vary from 0 to 0.5. Also $d_2' = 0.5 - d_2, d_1' = 0.5 - d_1$, C_{R1} and C_{R2} are row1 and row2 in state matrix C. $C_{mode1R1}, C_{mode2R2}$ etc are the second row matrices in Mode-1, Mode-2 etc. Assuming that $d_1 = d_2 =$ d, the state space model then gets modified as
$\frac{d\hat{x}(t)}{dt} = A\hat{x}(t) + B\hat{u}(t) + [(A_1 - A_2)X + (A_3 - A_4)X + (B_1 - B_2)U +$
$(B_3 - B_4)U]\hat{d}(t)$

In this converter $B_1 = B_2 = B_3 = B_4$,$C_1 = C_2 = C_3 = C_4$, the state equation in s-domain is

$$\hat{x}(s) = (sI - A)^{-1}B\hat{u}(s) + (sI - A)^{-1}((A_1 - A_2)X + (A_3 - A_4)X) * \hat{d}(s) \tag{5.13}$$

And $E_1 = E_2 = E_3 = E_3 = 0$, the output equation is $\hat{y}(s) = C\hat{x}(s)$ Taking $\hat{u}(s) = 0$ for constant input voltage hence the transfer function of output to duty ratio $\hat{d}(s)$ can be modified as in equation (5.14)

$$\hat{y}(s) = C(sI - A)^{-1}((A_1 - A_2)X + (A_3 - A_4)X) * \hat{d}(s) \tag{5.14}$$

The output voltage from second row of matrix (Appendix B.1) is given by the equation (5.15).

$$\hat{v_o}(s) = C_{R2}(sI - A)^{-1}((A_1 - A_2) + (A_3 - A_4))X * \hat{d}(s) \quad (5.15)$$

The transfer function of output voltage to duty ratio is given by the Eqn. 5.16.

$$G_p(s) = \frac{\hat{v_o}(s)}{\hat{d}(s)} = C_{R2}(sI - A)^{-1}[(A_1 - A_2) + (A_3 - A_4)]X \quad (5.16)$$

where $\hat{d}(s)$ and $\hat{v_o}(s)$ are small perturbations in the duty ratio and output voltage respectively bound to their steady state values d and V_o. (In practical designs, the variation of duty ratio d_1 for switch S_1 and d_2 for switch S_2 are limited to 50%, hence peak current of the switches get reduced considerably.)

From Appendix B.1, the matrices A_1 - A_2 and A_3 - A_4 are evaluated as given below

A_1 - A_2 =

$$\begin{bmatrix} \frac{r_{c1}}{L_{1a}} & 0 & 0 & 0 & \frac{1}{L_{1a}} & 0 & 0 & 0 \\ 0 & \frac{r_{c1}}{L_{1b}} & 0 & 0 & \frac{1}{L_{1b}} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\frac{1}{C_1} & -\frac{1}{C_1} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

A_3 - A_4 =

$$\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{r_{c2}}{L_{2a}} & 0 & 0 & \frac{1}{L_{2a}} & 0 & 0 \\ 0 & 0 & 0 & \frac{r_{c2}}{L_{2b}} & 0 & -\frac{1}{L_{2b}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_2} & \frac{1}{C_2} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

By substituting values from Table (5.1) in the equation (5.16) and multiplying also with modulator transfer function (G_m(s) =0.39, refer section 3.5) then the open loop transfer function in s-domain is given by Eqn. (5.17).

$$G_p G_m(s) = \frac{(b_1 s^7 + b_2 s^6 + b_3 s^5 + b_4 s^4 + b_5 s^3 + b_6 s^2 + b_7 s + b_8)}{(s^8 + a_1 s^7 + a_2 s^6 + a_3 s^5 + a_4 s^4 + a_5 s^3 + a_6 s^2 + a_7 s + a_8)} \tag{5.17}$$

where $b_1 = 8.32, b_2 = 8.32 * 10^8, b_3 = 2.08 * 10^{16}, b_4 = -2.812 * 10^{18}$, $b_5 = 1.012 * 10^{24}, b_6 = -4.712 * 10^{25}, b_7 = 1.227 * 10^{31}, b_8 = 4.07 * 10^{32}$ $a_1 = 5 * 10^7, a_2 = 7.996 * 10^{08}, a_3 = 5.645 * 10^{15}, a_4 = 2.095 * 10^{17}$, $a_5 = 1.804 * 10^{23}, a_6 = 6.965 * 10^{24}, a_7 = 1.771 * 10^{30}, a_8 = 5.882 * 10^{31}$.

The bode plot of the plant transfer function 5.17 is shown in Fig. (5.6).

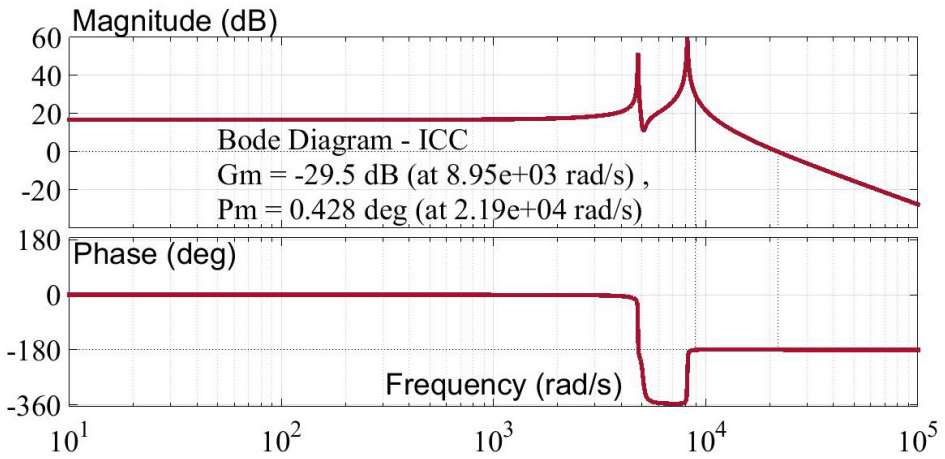


Fig. 5.6: Bode Plot of open loop ICC with modulator

5.6 Design of Type III Compensator

The phase margin is very low and the phase lag is to be up lifted by a type III compensator, similar to section 3.5.1 for closed loop voltage mode duty ratio control. The transfer function of the designed type III compensator is given in the Eqn. (5.18),

$$G_c(s) = 2.65 * 10^5 * \frac{s^2 + 2 * 3952.1s + 3952.1^2}{s(s^2 + 2 * 77490s + 77490^2)} \tag{5.18}$$

which is used in digital controller for simulation and practical validation. The convolution of equations 5.17 and 5.18 provide overall transfer function of the compensated closed loop system. The bode plot of the compensated system of ICC is shown in Fig. 5.7. The complete closed loop system of ICC is stable with a phase margin of 38.9° and gain margin of 16.5 dB. This type III is compensator is used to produce PSPWM for triggering the switches

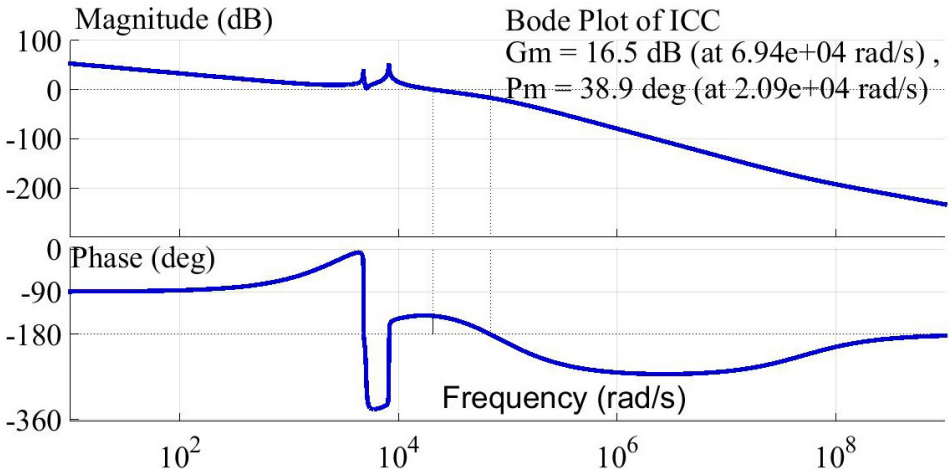


Fig. 5.7: Bode plot of closed loop compensated system of ICC with phase margin = 38.9°

of ICC in closed loop. The amplitude of compensator output is reduced to half, then this dc voltage is compared with triangular signal to generate PWM for the switch S_1. The pulse for switch S_2 is generated by phase shifting the pulse train of first PWM. Fig. 5.8 shows the realization scheme in closed loop, this scheme is simulated in the section to follow:

5.7 Simulation of Proposed ICC in Closed Loop

The Proposed ICC is simulated in closed loop with designed values as shown in Table 5.1. The parasitic values of inductors and capacitors are also considered while conducting simulation in

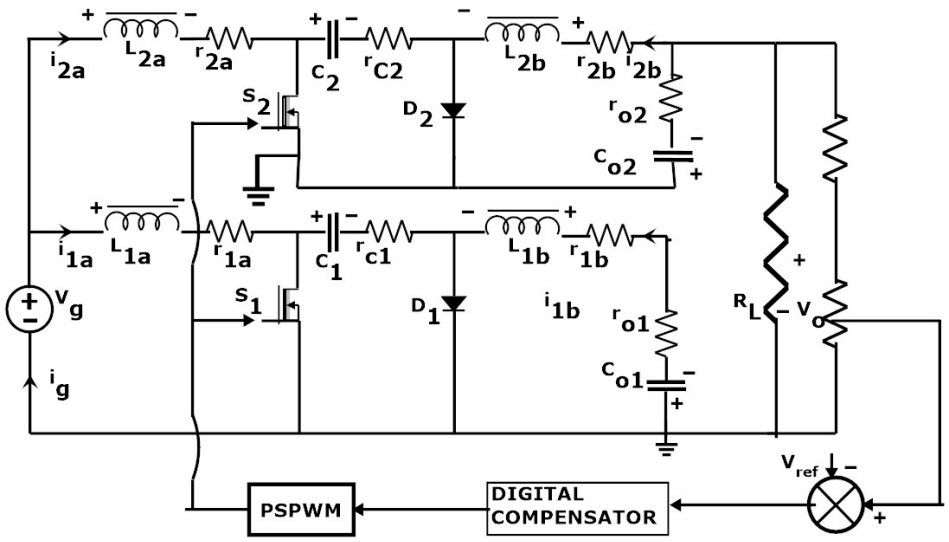


Fig. 5.8: Block diagram for closed loop operation of the Proposed ICC for simulation using type III compensator

MATLAB. In general is seen that the output voltage transient is very low and the the ripple contents on load voltage and load current are also low. The simulation scheme analyses the operation of Proposed ICC in continuous conduction mode. Both output voltage and output current are negative and hence the product is positive. Hence converter is shown to operate in quadrant III, drawing power from the source.

In the closed loop scheme, the output voltage is compared with set value of -15V corresponding to a duty ratio d $=d_1 = d_2 = 0.43$, $0 <$ d < 0.5. The error is processed in a type III digital compensator which gives a DC signal, which in turn is compared with carrier signal to generate the pulse train for triggering the switches at 25kHz.

5.8 Results and Discussions

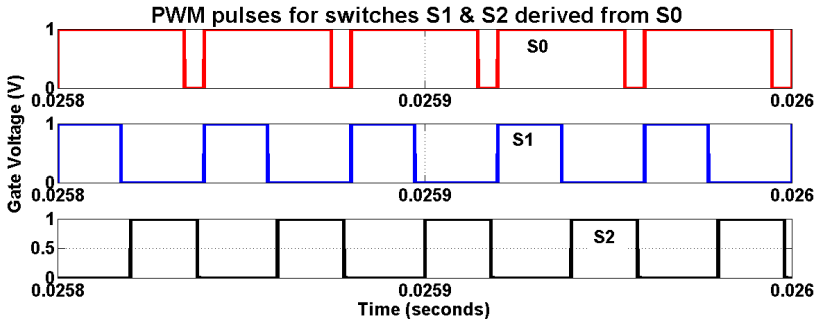


Fig. 5.9: The PSPWM scheme generated by closed loop control: S0 - PWM for switch in CCC, S1 and S2 -PSPWM for switches S_1 and S_2 of Proposed ICC

The pulse train is generated with a duty cycle of $d = 0.43$ in closed loop. The pulses generated in closed loop from simulation is shown in Fig. 5.9. The ON time of PWM pulse (refer Fig.5.2) is divided to two equal halves and which is used to turn ON the switches. Referring to Fig.5.8, the pulse is applied to the first switch S_1 and a phase shifted pulse is applied to the second switch S_2. It is thus ensured that both switches will never turn ON together. The OFF time is also divided into two halves and which is used for conductions of respective diodes D_1 and D_2. Referring to the timing diagram Fig. 5.2, the switches are turned ON, one at a time, for a period of $T_{ON}/2$. After $T_{ON}/2$ period both switches are in OFF position for the duration $T_{OFF}/2$. At this time diode D_1 connected to the first switch circuit also conducts along with the other diode D_2 which was previously conducting. After T/2 the second switch S_2 is turned ON for $T_{ON}/2$ period (and S_1 remains in OFF position). Thereafter both switches are again OFF when the diode D_2 of second switch circuit becomes forward biased. It can be

observed from the waveforms in Fig.5.9 that both switches are not ON together and there exists common OFF time for the switches.

The major performance indicators of the Proposed ICC are summarized below from the measurement carried out on the simulation:

5.8.1 Voltage

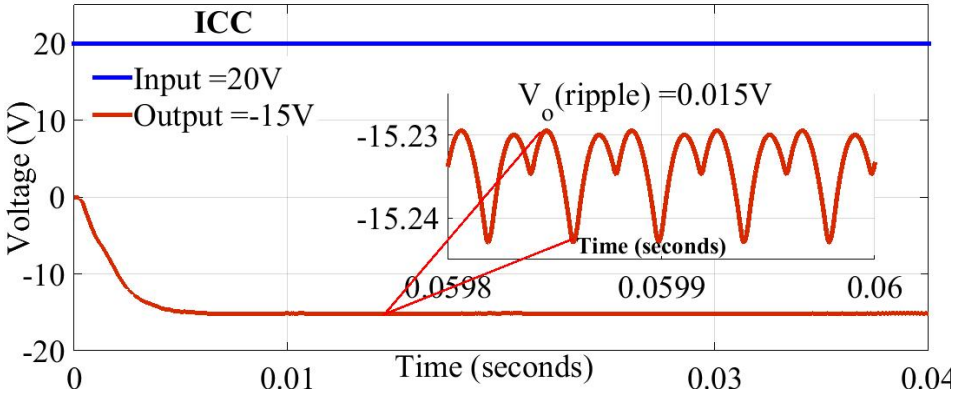


Fig. 5.10: Input voltage and Output voltage of Proposed ICC, the ripple on output voltage V_o(ripple)=0.015V (1%)

The output of the Proposed ICC measured is shown in Fig.5.10. The measured value of output voltage is -15V for an input voltage of 20V. From the waveform shown in Fig.5.10, it can be seen that ripple content on output voltage is very low. The settling time is approximately 5ms and overshoot is nil. (The settling time of the interleaved boost converter is 0.4 seconds [9]). The percentage of ripple is 0.1% in the Proposed ICC, which is very much less compared to 1.2% in case of CCC.

5.8.2 Current

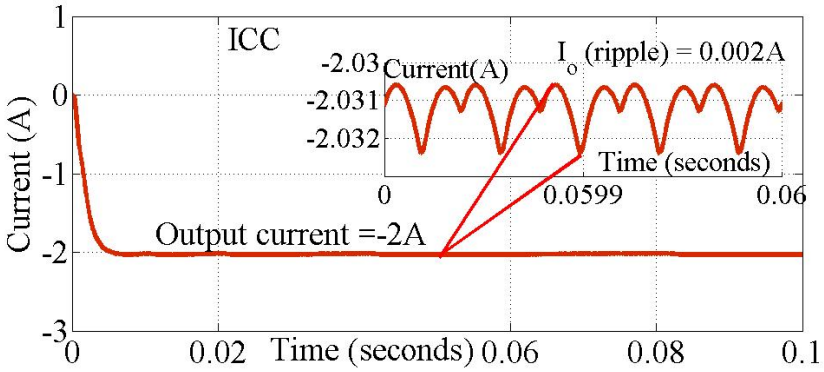


Fig. 5.11: The output current waveform of Proposed ICC in closed loop, $I_o = 2A$, the ripple on output current $I_o(rip)$ =0.002A

The output current shown in Fig. 5.11 indicates a low amount of ripple content. The output current of -2A is measured for an output resistor of 7.5Ω. As expected the Proposed ICC provides negative output current. The ripple on output current is also shown in Fig. 5.11, which is only 0.1% as against the ripple obtained in the case of simulation result of the CCC, where the ripple was 1.2%)

The waveforms of the current drawn from the source are shown in Fig. 5.12. The input source current of 1.65A is seen to be drawn from the source, to produce the required out current of -2A at -15 V. It is interesting to see that the average value of inductor currents I_{1a} and I_{2a} are 0.875A each The inductor current waveforms have ripple of 0.45A, which is similar to that of the CCC. But with the proposed interleaved feature, the source current ripple has been brought down further to 0.125A. The ripple on source current is thus 7.2% only, in contrast to the o 27% of ripple content in CCC.

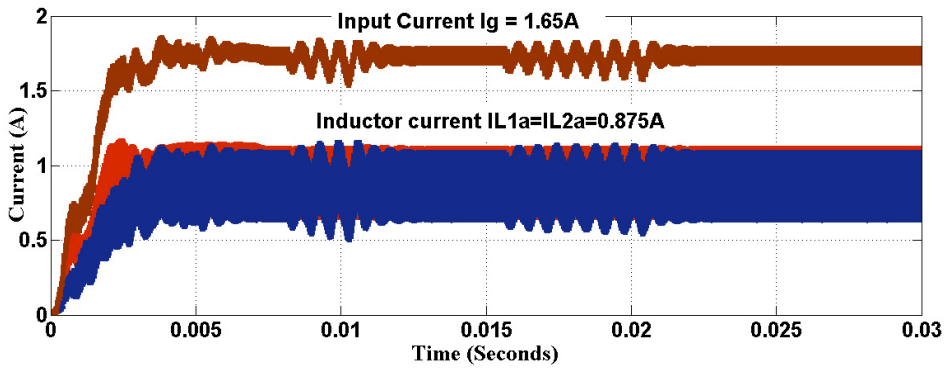


Fig. 5.12: Source current and inductor current wave form for Proposed ICC

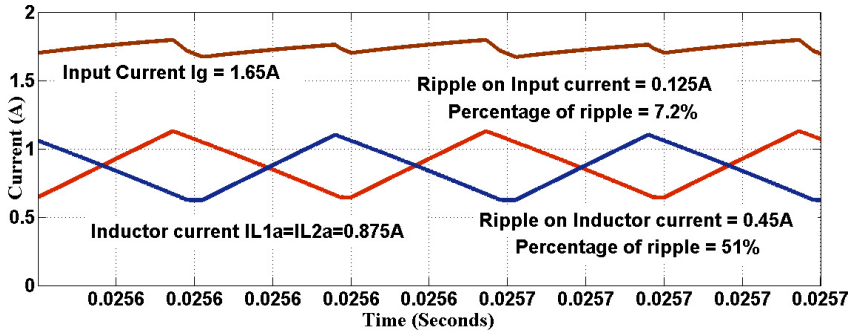


Fig. 5.13: Ripple on source current and inductor current waveform for Proposed ICC

The waveform of the ripple current alone shown in Fig.5.13 underscores the superior performance of the Proposed ICC.

A current measurement block is inserted in series with MOSFET to measure switching current. The switching current measured is shown in Fig. 5.14. It can be seen that the peak current of switch in the

proposed ICC is two times the load current (I_o = -2A) for an output voltage of -15V and is admirably less lesser than that in the switch current of CCC.

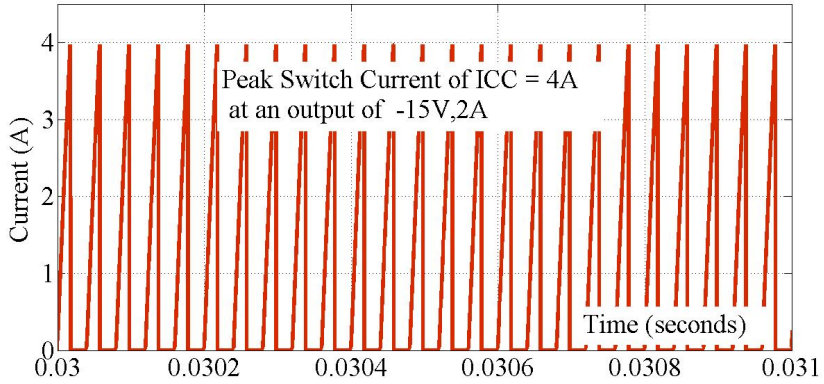


Fig. 5.14: Switch current waveform for Proposed ICC

5.8.3 Transients

In order to study the effect of sudden variation in the input voltage, the line transient is measured by changing input voltage from 17V to 23V at 15ms, after the start of simulation. The reference of the output voltage was set to -12V. It was observed (Fig. 5.15a) that the output voltage settles to set voltage of -12V, after a small transient settling time of 5 ms with an overshoot is only 2 V. Noting that transient can happen in response to the changes in input voltage as well as the load current, the load transient is also measured by changing load current from -1A to -2A at 15 ms. Here again the output voltage reference point is set to -12V. It was observed (from Fig. 5.15 b) that the output

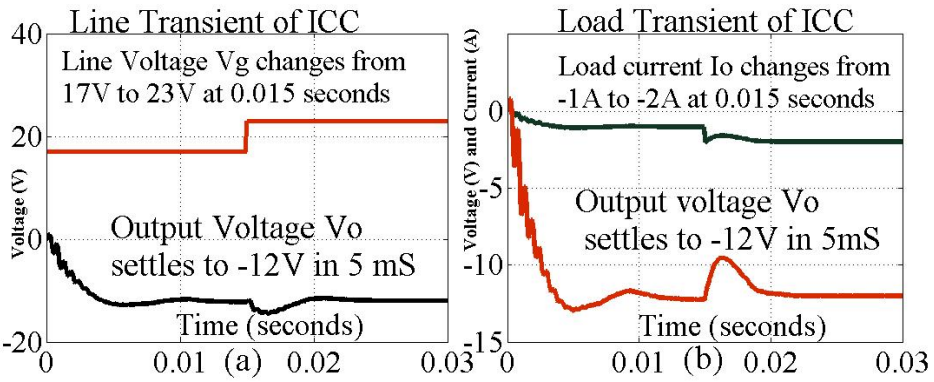


Fig. 5.15: Line transient of V_g in Proposed ICC changes from 17V to 23V at 15ms, Output voltage settles to -12V in 5ms,
Load transient of Proposed ICC I_o changes from -1A to -2A at 15 ms , Output voltage settles to -12V in 8ms

voltage settles to -12 V after a small transient settling time of 5 ms. The transient under shoot is only about 3 V.

5.9 Summary

The chapter repots the development of the Proposed Interleaved Cuk Converter (Proposed ICC). The design is systematically evolved and simulated using MATLAB in closed loop using type III compensator, by maintaining the output voltage constant for line voltage changes and load current variations. In order to maintain the load current and output voltage, a digital z-domain compensator is designed and implemented in the closed loop simulation. The design brings out notable advantages against the CCC in respect of low switching stress, stable output voltage and load current and admirably low

ripple at the input current and output voltage. The performance improvement as above is convincingly demonstrated in the plots given in Fig 5.9 to Fig. 5.15. The quick settling time, low over and undershoot during transient behaviour also underscores the improvement in the design of Proposed ICC. The findings from this chapter is published [83] to substantiate analysis and development of circuits towards Proposed ICC. The detailed hardware realization of the Proposed ICC is presented in the chapter 6 to follow.

Chapter 6

Hardware Realization of Proposed Interleaved Cuk Converter

6.1 Introduction

The Proposed ICC introduced and simulated in detail in chapter 5 has been realized in hardware, which is discussed in the present Chapter. All the components required for realization viz. the inductors and capacitors are designed based on ripple current and voltage similar to those in CCC (in Chapter 4). Current sensors LA55P is used to measure source, inductor and output currents. The measured current is scaled down as 1A=1V and plotted using 100MHz DSO. The output voltage is scaled down by forming potential divider circuit, as required.

The Modified ICC along with FPGA digital controller is shown in Fig.6.1. While realizing the hardware, the reference voltage is given

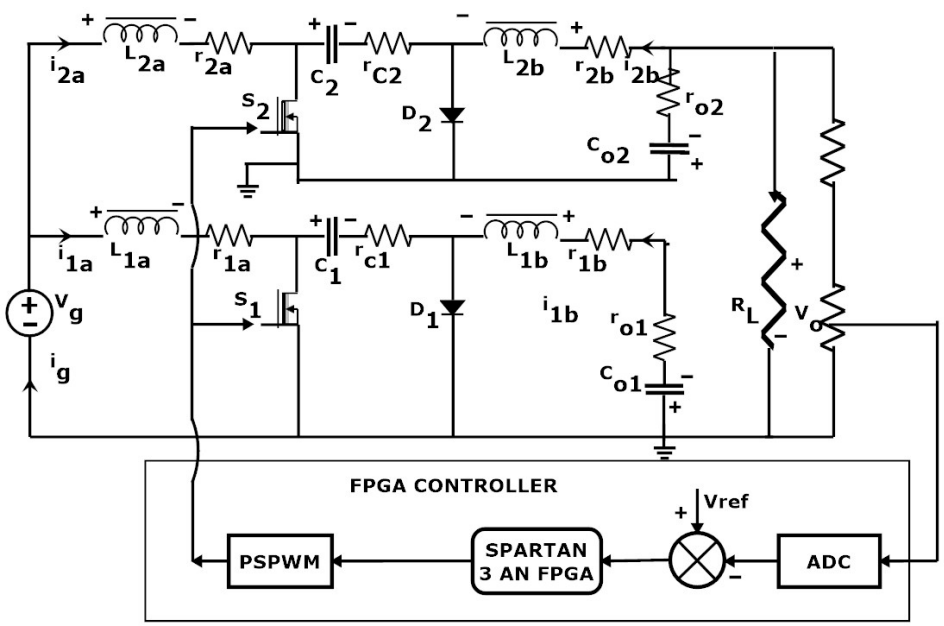


Fig. 6.1: Block diagram for closed loop operation of Proposed ICC for hardware

as hexadecimal value in SPARTAN 3-AN FPGA controller, where the output voltage is taken as feedback the inbuilt ADC. The output voltage is scaled down to a limited value of 3.3V suitable to ADC of the controller.

The feedback voltage is compared with digital reference voltage to generate error. The error is processed in a digital type III compensator, emulated in FPGA controller using XILINX tool. The DC output of compensator is compared with triangular signal to generate the PSPWM required for switching. Thereafter, the PSPWM is level shifted up using driver circuit to meet the hardware requirements of realization.

6.2 Selection of Components

As in the case of the hardware realization of CCC, discussed in Chapter 4, the passive components were designed following the standard approach. Table 6.1 summarizes the values of components, that were arrived in Chapter 5 for realizing the Proposed ICC for 80W output. It may be noted that while standard values of capacitors are taken, the inductor is realized by winding the SWG copper wire on E-55 core to get required value of inductance.

Table 6.1: Designed values for the closed loop control of ICC

parameter	Values	parameter	Values
V_g	20 V	V_o	-40 V
$L_{1a} = L_{2a}$	0.38mH	$L_{1b} = L_{2b}$	0.75mH
$C_1 = C_2$	10uF	$C_{o1} = C_{o2}$	22uF
R_L	7.5 Ω	f_s	25 kHz

It can be seen from Table 6.1 that the practical values used for C_{o1} and C_{o2} are 22 μF, in deviation to the designed values arrived in Sec. 5.4.2. Referring to Fig. 6.1, the number of turns are designed [81] for $L_{1a} = 0.38$mH and $L_{1b} = 0.75mH$ as follows. The area product of the core is given by the equation (6.1).

$$A_p = A_c * A_w = \frac{LI_pI_{rms}}{k_wB_mJ} \tag{6.1}$$

where A_c - Area of core (mm^2), A_w - Area of window(mm^2).
L - Inductance in (H), I_p -Peak current (A), k_w=window factor
I_{rms} -RMS current (A) J - Current density, B_m - Maximum flux density
The number of turns (N) of wire required to be wound to get the required inductance $L_{1a} = 0.38$mH, is given by the standard formula,

$$N = \sqrt{\frac{L_{1a} * l_g}{\mu_o * \mu_r * A}} \tag{6.2}$$

where l_g = length of air gap of the core, $\mu = \mu_o\mu_r$ = permeability and A_p is given in Eqn. 6.2. For the value of I_p is taken as 5A, I_{rms} = 3.54 A. Assuming current density J = 3A/ m^2, K_w = 1mm, B_m = 0.3T, the area of conductor to be wound is given by a_c = 3.54/3 = 1.18 mm^2. Choosing the SWG 22 wire, the conductor gives an area of 0.397 mm^2 and so 3 wires are wound to realize the area of 1.18 mm^2. The present design has used the standard value of the area of the core, from the data sheet [84], for the ferrite core E-55 to get A_p = 353 * 10-6 mm2, (instead of using Eqn. 6.1). Finally, choosing l_g = 1mm, the number of turns is calculated from Eqn. 6.3, as N = 29, to give the required inductance value of 0.38 mH.

$$N = \sqrt{\frac{0.38 * 10^{-3} * 1 * 10^{-3}}{4\pi 10^{-7} * 353 * 10^{-6}}} = 29 Turns \tag{6.3}$$

Similarly, the inductance of L_{1b} = 0.75 mH, the number of turn works out to be 42.

$$N = \sqrt{\frac{0.75 * 10^{-3} * 1 * 10^{-3}}{4\pi 10^{-7} * 353 * 10^{-6}}} = 42 Turns \tag{6.4}$$

6.3 Hardware Realization of the Proposed ICC

The photograph of hardware is shown in Fig. 6.2.

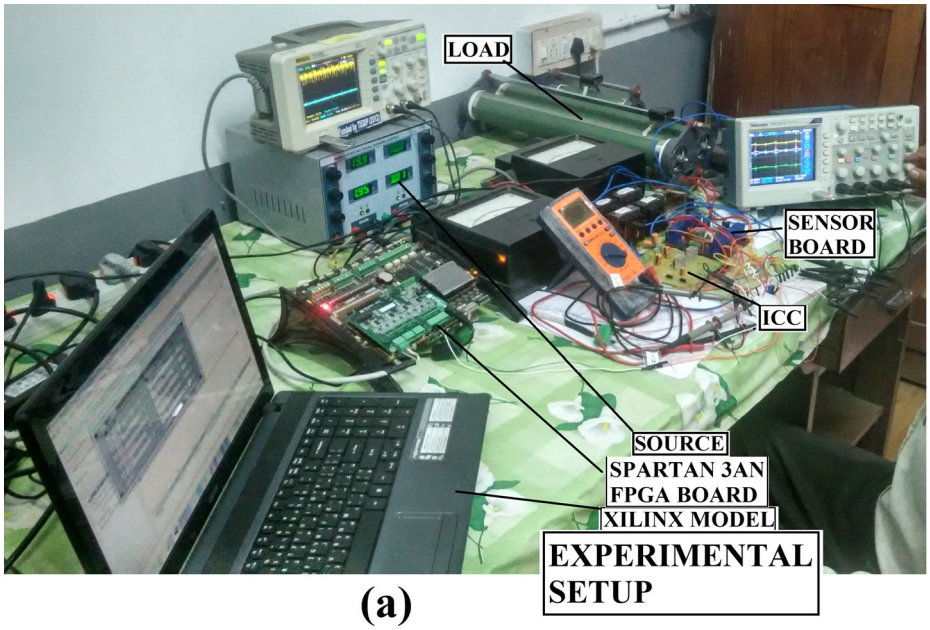


Fig. 6.2: Photo: Experimental setup of Proposed ICC along with Altium FPGA board and XILINX software

A 30V, 5A DC source is used to give an input voltage of 20V to the circuit of Proposed ICC. A 100Ω, 5A variable rheostat is used along with SPST mechanical switch to measure the load transient. The rheostat is varied to note the observations at different load currents by keeping the DC source voltage constant.

Standard instruments like digital multimeter, analog ammeters, analog voltmeters and DSO are used to take the observations from the circuit realized. Also the current is measured by the sensor the circuit prepared using LA55P sensor.

6.4 Measurements from Hardware Realized at an Output -15V, - 2A

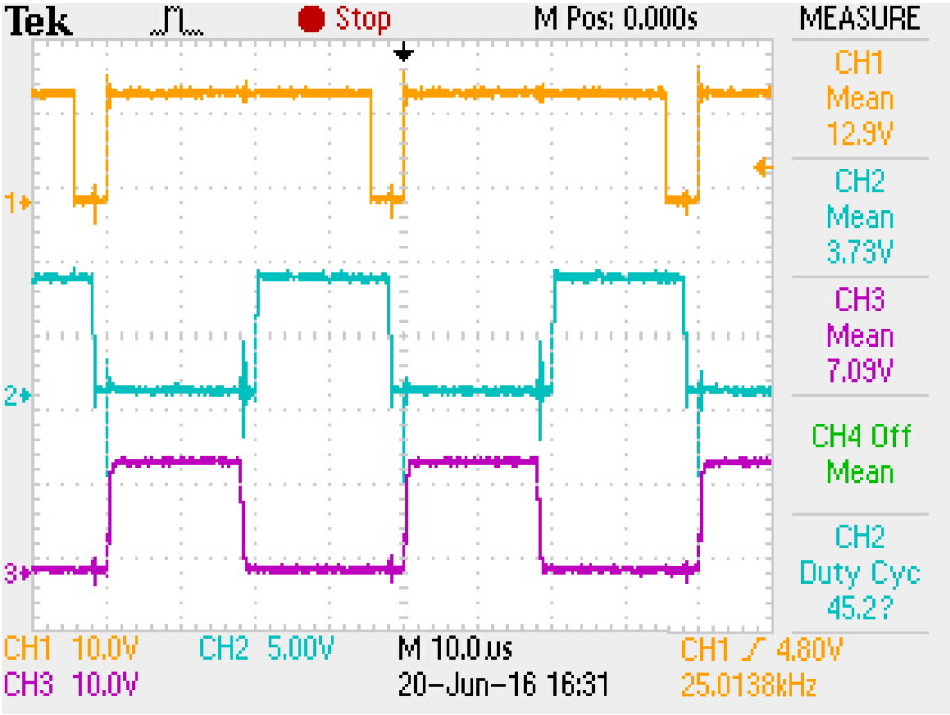


Fig. 6.3: PSPWM generated in hardware set-up for ICC

The PWM pulse required for switching is derived from the deviation of the voltage fed back from output and the reference voltage set. For this, the feedback voltage is scaled to a ratio of 10kΩ/100kΩ and is given to the input of ADC of FPGA controller. The reference voltage is entered manually in hexadecimal code to the controller. The type III compensator designed in Sec. 5.5, is realized in the

FPGA modulator to process the error required to produce the PWM pulse train. The PWM pulse train is divided to two halves and is applied to two switches, in order to alternatively trigger ON switches in either legs of the Proposed ICC. The Phase Shifted PWM pulse is shown in Fig. 6.3.

The performance of the hardware realized is assessed by observing

1. the voltages and currents at the input and output ,
2. the switching stress
3. transient behaviour and
4. over all efficiency,

there by confirming the association with the simulation.

6.4.1 Voltage

The proposed ICC is tested by applying an input voltage of 20V (from a 30V, 5A power supply). The steady state output voltage measured on the oscilloscope is shown in Fig. 6.4 as -15V (in red) at output load current of -2A. The input voltage of 20 V is shown in blue. However, on a finer measurement scale, it is seen that the output voltage has a certain amount of ripple. As shown in Fig. 6.4 (in the inset), the ripple on output voltage of -15V, at a load current -2A is measured as 400mV, which is works out to be 2.7% which is very less than in comparison with the CCC. In the case of CCC, ripple was 700mV, i.e. 4.5% under similar conditions.

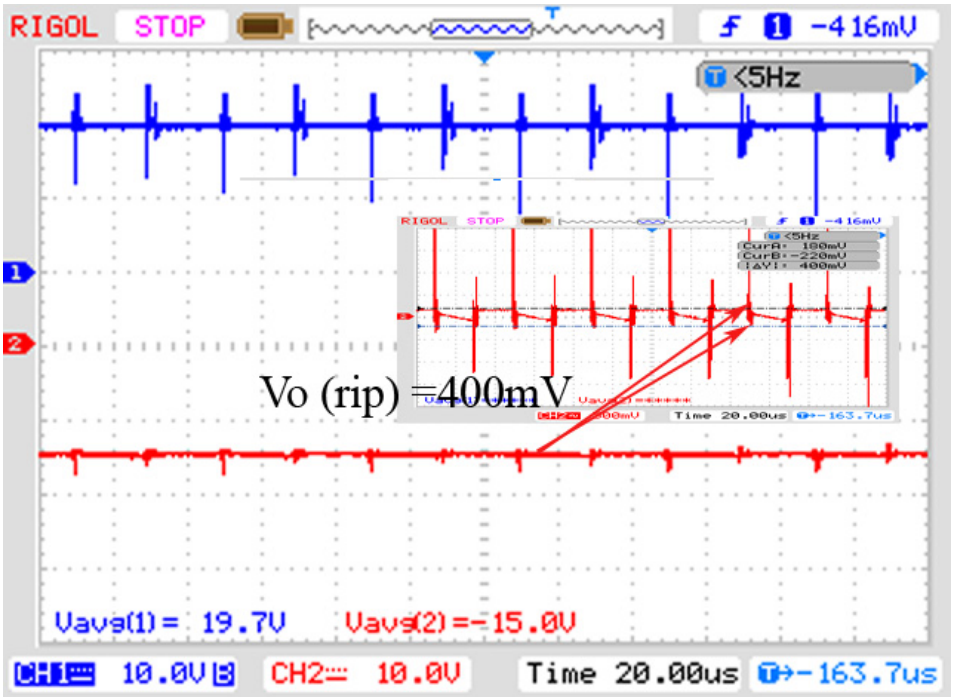


Fig. 6.4: For the input voltage of 20V (shown as blue), the steady state output voltage is measured as -15V (in red) at -2A output load current, Ripple content on output voltage of ICC (shown as red in inset) at -15V is 400mV

6.4.2 Current

The waveform of the input and output current are shown in Fig. 6.5. With a resistive load of 7.5Ω connected across -15V output, the converter produces an output current of -2A, while drawing an input current of 1.83A. Current sensors are used to measure input and output currents. For this the current sensor is scaled to measure 1A as 1V on the Oscilloscope . The ripple on the output current shown

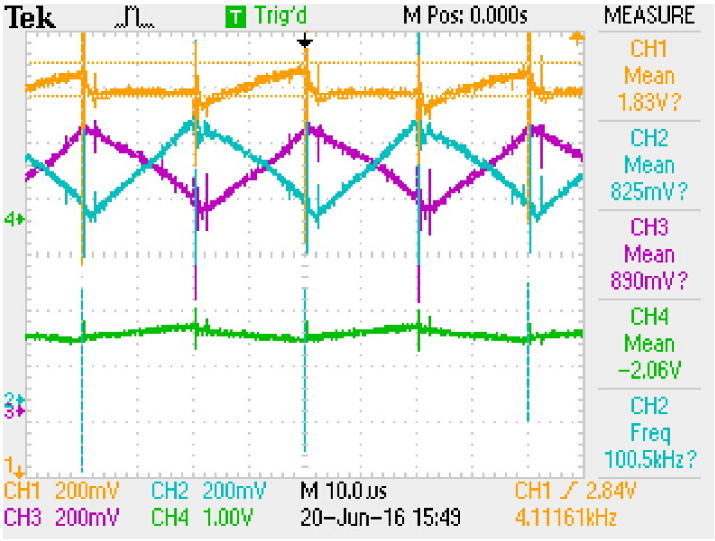


Fig. 6.5: Input(amber), input inductor (blue and violet) and output (green) currents of ICC

in Fig. 6.5 measures as 100mA (in green), which is 5% (0.1/2) at the measured output current of -2A. This also may be contrasted with the ripple on the output current of CCC. The ripple for the corresponding input current of 1.83A is 100mA (in amber), which is 5.5% (0.12/1.8) of the measured current. Hence the ripple on the source current has substantially come down from 400mA (27% in CCC) to 100mA, 5.5%in the proposed ICC. It is interesting to note that the individual inductor current still remain at 400mA.

The switch current of Proposed ICC, primarily responsible for energy transfer from input to output, is shown in Fig.6.6. The switching pulse train has a period of 40 μs and a pulse width of 18 μs for the switches S_1 and S_2. The peak value of switch current of ICC as observed in DSO is 4A at an output of -15V, -2A, which is twice the value of load

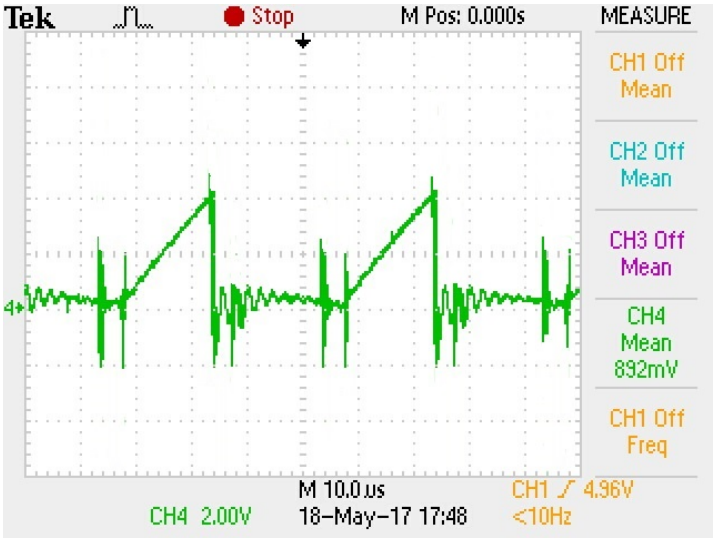


Fig. 6.6: Switch Current of Proposed ICC. The maximum value is 4A

current. However, it can be seen that the switch current of Proposed ICC is 38% lower than that of CCC. The reduction in switch current helps to reduce the size of the switching devices and also simplify the cooling arrangements.

6.4.3 Transients

Fig. 6.7 illustrates the transient behaviour of the Proposed ICC. The response of the Proposed ICC in the closed loop, to input line transient is measured by suddenly applying input voltage of 20V (in red). It can be seen that the output voltage (in blue) settles to the set value of -15V, within a settling time of 4ms without any overshoot. On the other hand the settling time is 125ms in CCC, which reconfirms the improved performance of the Proposed ICC.

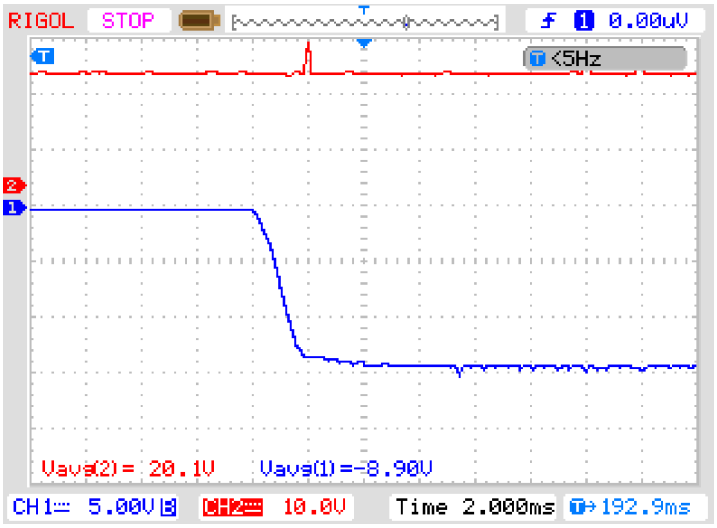


Fig. 6.7: Line transient of ICC at an output of -15V

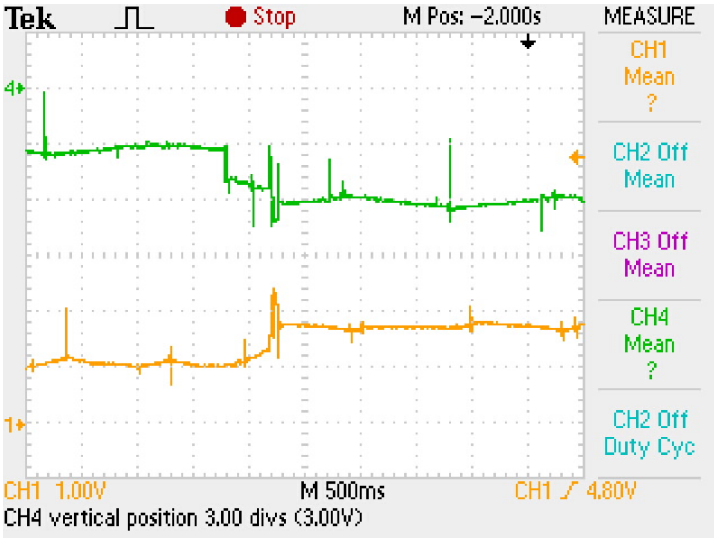


Fig. 6.8: load transient of ICC, in terms of output and input currents

The transient behaviour as seen from the load side is shown in Fig. 6.8. The load current (in green) has a change from -1A to -2.0A and input current (in amber) made a change from 1A to 1.8A. The settling time is approximately 125ms.

6.4.4 Efficiency

The measurement values of input and output voltages and currents are tabulated in Table 6.2. In order to plot the efficiency curve over a

Table 6.2: Efficiency of ICC converter at $f_s = 25kHz$

V_g (V)	I_g (A)	V_o (V)	I_o (A)	Effi (%)
20.1	0.34	-12	-0.5	87
20	0.7	-12	-1.04	88.6
20	1.01	-12	-1.59	94.1
20	1.27	-12	-1.98	93.5
20	1.66	-12	-2.6	93.97
20	1.92	-11.9	-3.03	92.9
20	2.22	-11.7	-3.5	92.2
20	2.75	-11.5	-4.2	87.8

range of load currents, the load current is varied from -0.5A to -4A, by keeping the input voltage constant. The output voltage, input current and output current are measured. The efficiency is calculated as the ratio of output power to input power. From the Table 6.2, it can be seen that the output voltage regulation is tight for the load current variations. The efficiency curve, shown in Fig.6.9, is nearly flat , with the highest efficiency being 94%. The average efficiency is found as 91% for Proposed ICC in practical validation. Table 6.3 brings out the correspondence of the facts mentioned in the simulations and hardware realization.

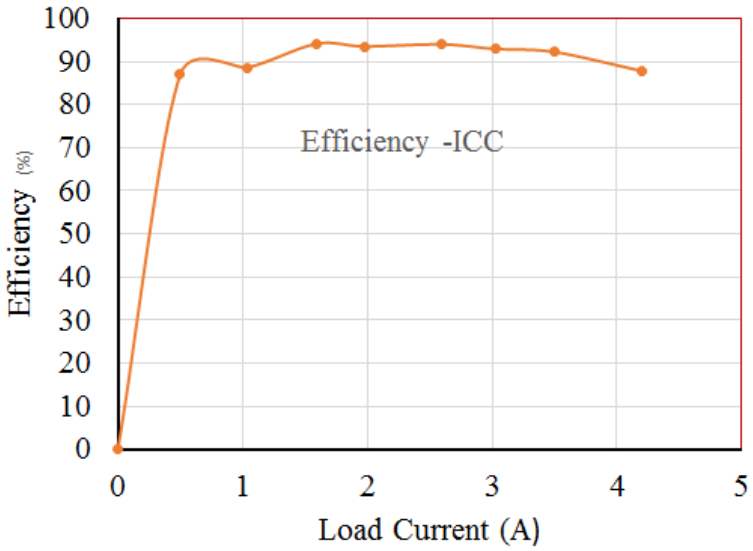


Fig. 6.9: Efficiency curve for ICC

Table 6.3: Results for Proposed ICC at $f_s = 25kHz$,d=0.43

parameter	Simulation Resutls	Experimental Results
V_g	20v	20v
V_o	-15v	-15v
I_g	1.7A	1.83A
I_o	-2A	-2.06A
I_{grip}	125mA (7.2%)	100mA (5.5%)
I_{orip}	2mA (0.1%)	100mA (5%)
V_{orip}	0.015V (0.1%)	0.4 (2.7%)
$I_{sw_{pk}}$	2.8A	4A
Line Transient	5ms	10ms
Load Transient	5ms	125ms
Efficiency	–	91%

In the Table 6.3 the parameters I_{grip}, I_{orip}, V_{orip} and $I_{sw_{pk}}$ respectively represents ripple on source current, ripple on output current, ripple on output voltage and peak value of switch current. The simulation and hardware results have slight variations in values since the parasitic resistance values for each energy storage elements are assumed in simulation, but actual values are practically considered in hardware validation.

The comparison with the Table 6.4 clearly underscores the improved performance of the Proposed ICC over the CCC, in respect of ripple currents, switch currents, line and load transients, though both the topologies offer similar behavior in respect of regulation and flatness of the efficiency curve.

Table 6.4: Comparison of CCC and Proposed ICC - Hardware at V_g = 20 V, V_o = -15 V, I_o = -2 A, I_g = 1.8 A, f_s = 25 kHz

Parameter	CCC	Proposed ICC
$I_{g(rip)}$	400 mA (22.2%)	100 mA (5.5%)
$V_{o(rip)}$	1.08 V(7%)	400mV (2.7%)
$I_{o(rip)}$	100 mA (5%)	100 mA (5%)
Line transient	125 mS	4 ms
Load transient	400 ms	125 ms
Efficiency	89%	91%

6.5 Summary

The present chapter has brought out the details of the hardware realization of the Proposed ICC, with the PSPWM switching

sequence, corresponding to buck mode of operation i.e. at -15V, -2A output. From the observations made out of detailed measurements of steady state and transient behaviour of both input and output voltages, it is demonstrated that the proposed design outperforms the CCC. It is interesting to note that the ripple content on the source side current is high about 5% for an output voltage of -15V, while the peak current of the switch is reduced by 31% when the converter operates with duty ratio less than 0.5. Further the efficiency is not sacrificed while attempting to reduce input current ripple. The average efficiency, over 91% is noted in hardware for the Proposed ICC, is high, which remains flat for an appreciable variation of load current. The findings from practical validation of Proposed ICC is published [85] - [86] to substantiate the simulation results. The converter characteristics of Proposed ICC is limited to buck operation due to ripple building issues, a modified topology is presented in the next chapter to address this issue and provide boost operation.

Chapter 7

Modification on Proposed Interleaved Cuk Converter

7.1 Introduction

Though a Conventional Cuk Converter (CCC) reduces ripple current on input and output sides compared to that of basic DC-DC converters following the viz. buck, boost and buck boost topologies, it is shown that the Proposed ICC, introduced in Chapter 5, achieves substantial reduction in ripple content and switching stress, of course for a duty ratio below 50%. But in the Proposed ICC also, the duty ratio above 50% required for boost operation does not yield adequate ripple cancellation and so results in ripple building issues because of increases of switching stress. Increase in switch stress in turn pushes up the temperature, demanding adequate cooling arrangement at extra cost. Naturally, this shortens the life of switch as well.

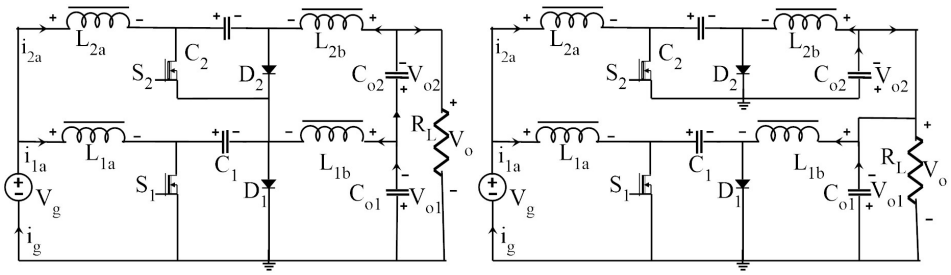
In order to achieve boost operation avoiding switching with duty ratio beyond 50%, a modified topology is proposed in the present Chapter. Accordingly, the output voltage will be sum of individual interleaved outputs. The Modified Interleaved Cuk Converter (Modified ICC) is demonstrated to overcome draw backs of ICC and its extensions introduced earlier in the thesis. The Modified ICC delivers a step-up of input voltage, while operating with a low duty ratio less than 0.5. Reducing the switching current noticeably, the converter is also capable of providing multiple output voltages with different magnitudes i.e. two outputs are directly from interleaved circuits and the third, which is greater than input voltage, is sum of these two interleaved outputs.

The reduction in switch current, which forms the crux of the development of the Modified ICC, comes from the PSPWM technique, used for triggering the switches. The PWM is divided into two halves so that the first switch is operated during first half cycle and second switch in second half cycle in Modified ICC. As a result, the switching current reset to zero on every ON time of half cycles thereby decreasing the rise of peak current of switch considerably in Modified ICC configuration. In contrast, in a CCC the switch is reset to zero on every ON time of the full cycles, throughout the circuit also uses the PWM technique .

7.2 Modified Interleaved Cuk Converter (Modified ICC)

As in the case of the proposed ICC, the Modified ICC, shown in Fig.7.1a, also consists of four inductors, four capacitors, two switches and two diodes, along with single DC source. The Proposed ICC

circuit (earlier shown in Fig. 5.1) is also shown in Fig. 7.1b for comparison, where the following components are directly grounded: the switch S_2, the Diode D_2 and the Capacitor $Co2$. In the Proposed ICC the output capacitors are parallel and they provide parallel output voltages with same magnitude. But in the Modified ICC



(a) Modified ICC circuit diagram developed from Proposed ICC

(b) Proposed ICC circuit diagram reproduced from Fig. 5.1

Fig. 7.1: Circuit diagrams of Proposed ICC and Modified ICC

shown in Fig. 7.1a, the second switch S_2 and second diode D_2, connected through S_1, touch the ground, only when S_1 is ON, or through D_1 otherwise. However, the first switch S_1 and the first diode D_1 are directly connected to the ground in the Modified ICC. As was indicated earlier in the Chapter 5, the PSPWM technique is used to trigger the switches S_1 and S_2.

In this circuit the input side is connected with a single source and the output side is connected in series to add up voltage across capacitors. As a result the modification on topology provides output voltage three times the input voltage at a duty ratio of 0.5. As the output filter capacitors are different potentials, they provide two variable output voltages. Thus the modified circuit provides three variable output voltages. The circuit operates identically in two half cycles of a given cycle. The detailed analysis of the Modified ICC,

shown in the Fig.7.1a, is carried out under ON and OFF conditions of switches as discussed below.

7.3 Derivation of Output Voltage of Modified ICC

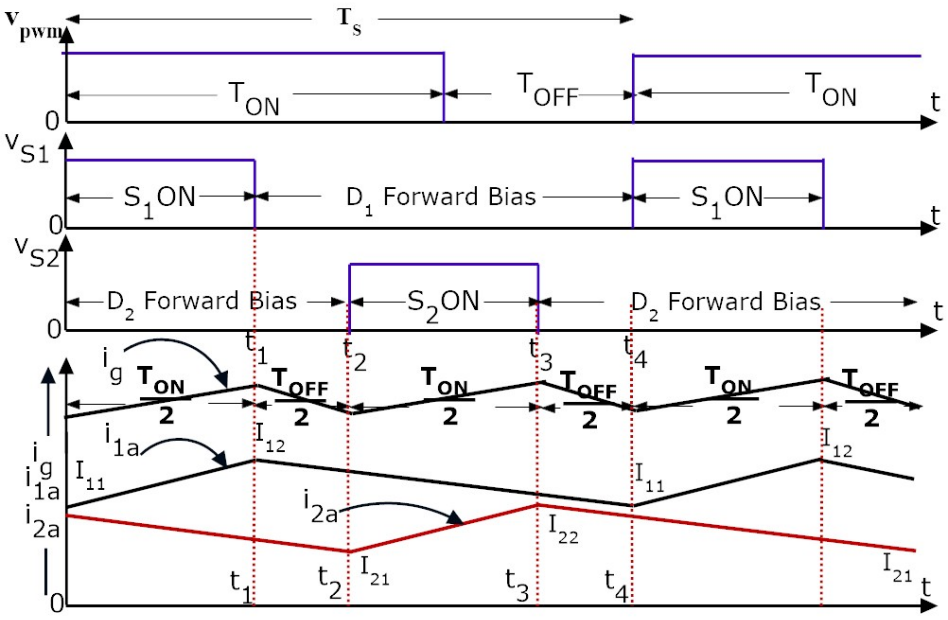


Fig. 7.2: Waveforms of PSPWM technique for Modified ICC: V_{PWM} = gate voltage of switch of CCC; V_{S1} and V_{S2} gate voltages of the two legs of Modified ICC; i_{1a} and i_{2a} : current through inductors L_{1a} and L_{2a}; i_g: source current of Modified ICC

The PSPWM scheme to trigger the switches S_1 and S_2 of Modified ICC is shown in Fig. 7.2. Also charging and discharging current of energy storage inductors along with source current waveform is shown. During $t_1 = d_1 T_s$ period (Fig.7.2), the switch S_1 is turned ON, when inductor current i_{1a} rises from initial value I_{11} and reaches to peak value I_{12}. At t_1 switch S_1 opens and inductor L_{1a} starts discharging from I_{12} through t_2 till the end of cycle t_4. Here the common OFF time is given by t_2 - $t_1 = (1 - d_1)T_s/2$. Similary on next half cycle, at t= t_2 switch S_2 is turned ON and inductor current i_{2a} rises from I_{21} and reaches to peak value I_{22}. At t = t_3 the switch S_2 opens and inductor L_{2a} starts discharging through t_4, here again the common OFF time is given by $t_4 - t_3 = (1 - d_2)T_s/2$. The cycle is thereafter repeated with PSPWM technique, such that $T_s = T_{ON} + T_{OFF}$. Here d_1 and d_2 represent duty ratios of switches S_1 and S_2 respectively for $0 < \{d_1, d_2\} < 0.5$.

The detailed operation of the circuit is discussed below in four modes (Refer Fig. 7.2). Initially the capacitor C_1 and C_{o2} are assumed as in charged state. Also assume that the filter inductor L_{1b} and energy storage inductor L_{2a} are in charged state.

7.3.1 Mode 1 - S_1 ON and S_2 OFF (t_o to t_1)

Fig. 7.3 illustrates the state of the circuit of the converter when switches S_1 is ON and S_2 is OFF. When inductor L_{1a} charges, at the same time inductor L_{2a} discharges, as shown in Fig.7.2. The capacitor C_1 discharges through S_1 in the circuit, completes with C_{o1}, L_{1b} and through the load R_L. The energy stored in the capacitor C_1 transfers to the load. The capacitor C_{o1} charges and L_{1b} discharges. Also C_{o2} discharges and hence L_{2b} charges. In this mode the previously charged inductor L_{2a} discharges and C_2 is charged.

Table 7.1: Status of elements during transition periods; FB- Forward Bias, RB-Reverse Bias.

Modes	**Status of Switch and Diodes**	**Period**	**Charging**	**Discharging**
Mode-1	S_1 ON, S_2 OFF D_1-RB, D_2-FB	t_0 to t_1	L_{1a}, L_{2b}, C_2, C_{o1}	C_1, C_{o2}, L_{2a}, L_{1b}
Mode-2	S_1 OFF, S_2 OFF D_1-FB, D_2-FB	t_1 to t_2	C_1, C_2, C_{02}, L_{1b}	L_{1a},L_{2a}, C_{o1}, L_{2b}
Mode-3	S_1 OFF, S_2 ON D_1-FB, D_2-RB	t_2 to t_3	L_{2a}, L_{1b}, C_1, C_{o2}	C_2, C_{o1}, L_{1a}, L_{2b}
Mode-4	S_1 OFF, S_2 OFF D_1-FB, D_2-FB	t_3 to t_4	C_1, C_2, C_{o2}, L_{1b}	L_{1a}, L_{2a}, C_{o1}, L_{2b}

The charging and discharging elements are shown in Table 7.1.

The voltage across inductors L_{1a}, L_{1b}, L_{2a} and L_{2b} is given by Eqn. (7.1).

$$\begin{aligned} L_{1a}\frac{di_{1a}}{dt} &= V_g \\ L_{1b}\frac{di_{1b}}{dt} &= V_{c1} - V_{o1} \\ L_{2a}\frac{di_{2a}}{dt} &= V_g + V_{c1} - V_{c2} \\ L_{2b}\frac{di_{2b}}{dt} &= V_{c1} - V_{o1} - V_{o2} \end{aligned} \tag{7.1}$$

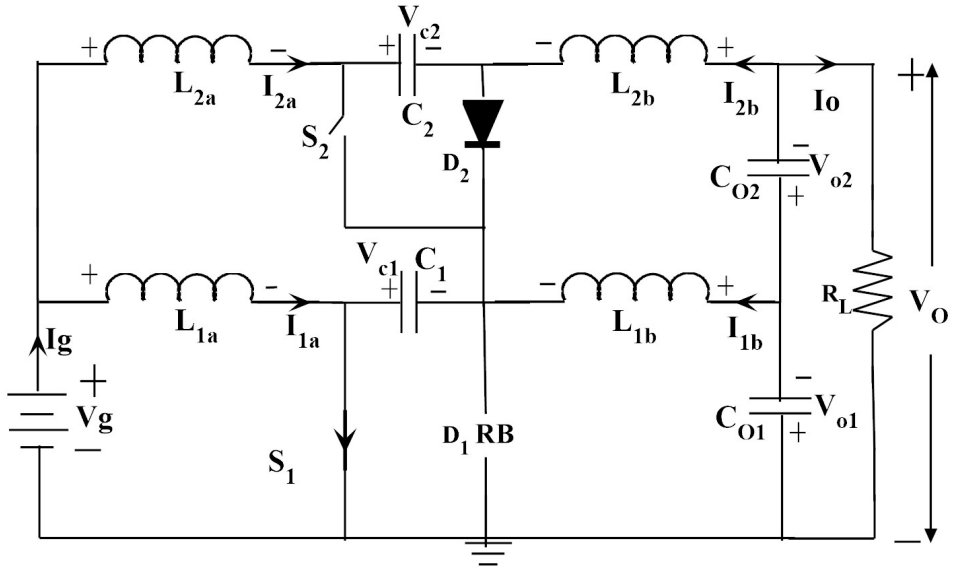


Fig. 7.3: Modified ICC circuit diagram when S_1 is ON and S_2 is OFF (D_1 RB : Diode 1 Reverse Biased)

7.3.2 Mode 2 - S_1 OFF and S_2 OFF $(t_1 - t_2)$

When both switches S_1 and S_2 are in OFF state as shown in Fig.7.4, both inductors L_{1a} and L_{2a} are discharging. The stored energy in inductors transfers to capacitors C_1 and C_2. So the capacitor C_{o1} discharges, which charges L_{1b} and C_{o2}. At the same time inductors L_{1b} and L_{2b} discharges as shown in Fig.7.2 and transfers energy to load. The charging and discharging elements are shown in Table 7.1.

The voltage across all inductors L_{1a}, L_{1b}, L_{2a} and L_{2b} are given by

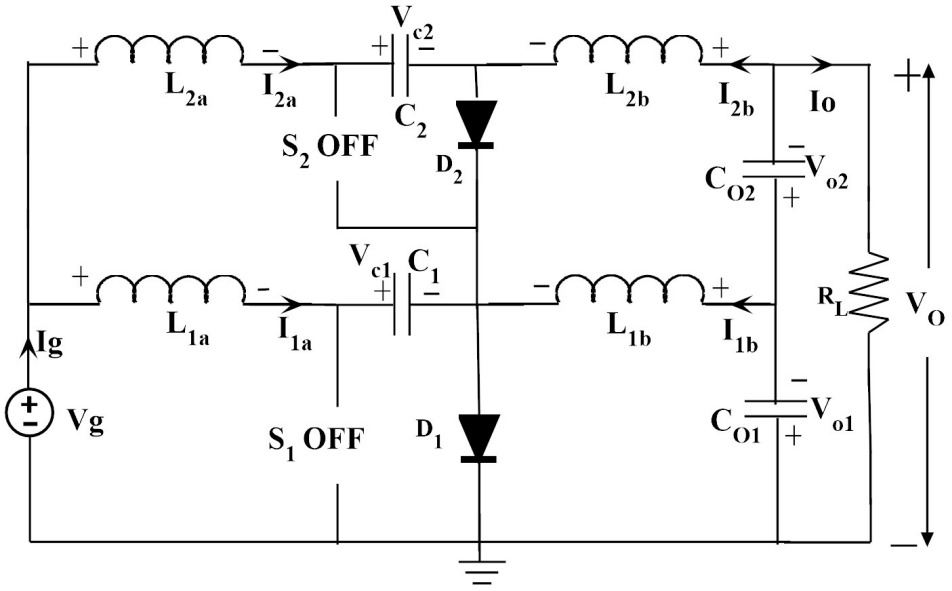


Fig. 7.4: Circuit diagram of Modified ICC when both switches are in OFF state

equations (7.2)

$$\begin{aligned} L_{1a}\frac{di_{1a}}{dt} &= V_g - V_{c1} \\ L_{1b}\frac{di_{1b}}{dt} &= -V_{o1} \\ L_{2a}\frac{di_{2a}}{dt} &= V_g - V_{c2} \\ L_{2b}\frac{di_{2b}}{dt} &= -V_{o1} - V_{o2} \end{aligned} \tag{7.2}$$

7.3.3 Mode 3 - S_1 OFF and S_2 ON $(t_2 - t_3)$

Fig. 7.5 illustrates the equivalent circuit of Mode 3. During this period, the charging and discharging process as shown in Table 7.1 takes place by closing the switch S_2. The charging elements are C_1, C_{o2}, L_{1b} and L_{2a}. Also the discharging elements are L_{1a}, C_{o1}, L_{2b} and C_2. As the switch S_2 is closed, the current through Inductor L_{2a} increases and it stores energy as shown in Fig.7.2. Also at the same time the transferring of stored energy from L_{1a} to C_1 continues and capacitor C_1 remains charging. The capacitor C_2 discharges through S_2, C_{o1}, L_{2b} and R_L, transferring the stored energy in the capacitor to the load.

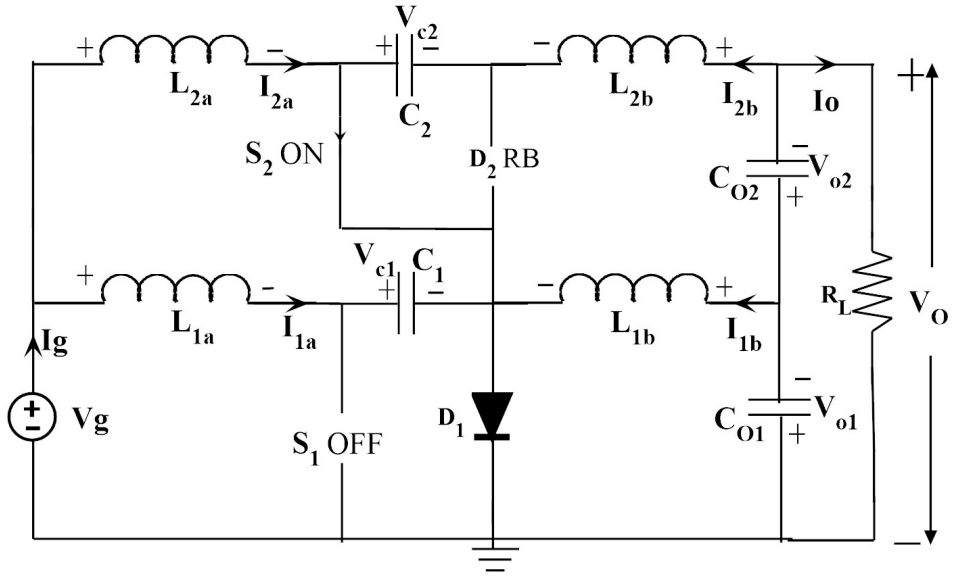


Fig. 7.5: Circuit diagram of Modified ICC when S_1 is OFF and S_2 is ON (D_2 RB: Diode 2 Reverse Biased)

The voltage across all inductors L_{1a}, L_{1b}, L_{2a} and L_{2b} is given Eqn. (7.3).

$$\begin{aligned} L_{1a}\frac{di_{1a}}{dt} &= V_g - V_{c1} \\ L_{1b}\frac{di_{1b}}{dt} &= -V_{o1} \\ L_{2a}\frac{di_{2a}}{dt} &= V_g \\ L_{2b}\frac{di_{2b}}{dt} &= V_{c2} - V_{o1} - V_{o2} \end{aligned} \tag{7.3}$$

7.3.4 Mode 4 - S_1 and S_2 OFF $(t_3 - t_4)$

When both switches are in OFF states, the circuit operates as shown in Fig.7.4. The operation is same as Sec. 7.3.2 and with this Mode, a switching cycle is completed. In this mode the charging and discharging, as illustrated by the waveforms of inductor currents, in Fig.7.2.

It may be noted that in any switching converters under steady state, the net change in inductor current over one complete switching period must be zero. Therefore the volt-sec balance to the inductor L_{1a} for the equations (7.1), (7.2) and (7.3) from Mode 1 to 4, is given by Eqn. (7.4)

$$V_g d_1 + (V_g - V_{c1})(0.5 - d_1) + (V_g - V_{c1})(d_2) + (V_g - V_{c1})(0.5 - d_2) = 0 \tag{7.4}$$

From the Eqn. (7.4),

$$V_{c1} = \frac{V_g}{(1 - d_1)} \tag{7.5}$$

From the relations of the voltage across inductor $L_{1b}d_{ib}/d_t$, described in all the four modes from Mode 1 to 4 (i.e from equations (7.1), (7.2) and (7.3)), the volt-sec balance is given by Eqn. (7.6)

$$(V_{c1} - V_{o1})d_1 - V_{o1}(0.5 - d_1) - V_{o1}(d_2) - (V_{o1})(0.5 - d_2) = 0 \quad (7.6)$$

Substituting the Eqn. (7.5) in equation(7.6) results one of the interleaved output voltage as in the Eqn. (7.7).

$$V_{o1} = \frac{d_1 V_g}{(1 - d_1)} \quad (7.7)$$

Similarly for inductor voltage equations (7.1), (7.2) and (7.3) from Mode1 to 4, the volt-sec balance is given by Eqn. (7.8)

$$(V_g + V_{c1} - V_{c2})d_1 + (V_g - V_{c2})(0.5 - d_1) + V_g(d_2) + (V_g - V_{c2})(0.5 - d_2) = 0 \quad (7.8)$$

Substituting Eqn. (7.5) in the Eqn. (7.8) to obtain voltage across capacitor C_2,

$$V_{c2} = \frac{V_g}{(1 - d_1)(1 - d_2)} \quad (7.9)$$

Further the equations (7.1), (7.2) and (7.3) for the inductor L_{2b}, from Mode1 to 4 yields the volt-sec balance as given in Eqn. (7.10)

$$(V_{c1} - V_{o1} - V_{o2})d_1 - (V_{o1} + V_{o2})(0.5 - d_1) + (V_{c2} - V_{o1} - V_{o2})(d_2) - (V_{o1} + V_{o2})(0.5 - d_2) = 0 \quad (7.10)$$

The second interleaved output voltage V_{o2}, as shown in Eqn. 7.11, is obtained after substituting equations (7.5), (7.7) and (7.9) in the Eqn. (7.10).

$$V_{o2} = \frac{V_g d_2}{(1 - d_1)(1 - d_2)} \quad (7.11)$$

Adding the two voltages V_{o1} and V_{o2}, results in the output voltage V_o of the Modified ICC circuit, given by the Eqn. (7.12).

$$V_o = -(V_{o1} + V_{o2}) \tag{7.12}$$

Substituting equations (7.7) and (7.11) in Eqn. (7.12), the expression for output voltage of Modified ICC is given by the Eqn. (7.13).

$$V_o = -\frac{d_1 V_g}{(1-d_1)} - \frac{d_2 V_g}{(1-d_1)(1-d_2)} \tag{7.13}$$

The Eqn. 7.13 can be controlled for constant output voltage V_o by varying duty ratios d_1 and d_2. The interleaved output voltages V_{o1} and V_{o2} are having different magnitudes according to the equations 7.7 and 7.11, but the Proposed ICC produces identical parallel outputs. The second phase interleaved circuit is connected to the ground through the switch S_1 or the diode D_1, which produces different magnitudes for two interleaved output voltages. Here the output capacitors are series and hence third output voltage is sum of two interleaved outputs. All three output voltages and currents with negative polarity, which falls into quadrant III operation. The buck and boost operations possible with output voltage Eqn. 7.13. Assume that $d_1 = d_2$=d, $0 <$ d < 0.5 then the Eqn. 7.13 can be modified as,

$$V_o = \frac{(d^2 - 2d)V_g}{(1-d)^2} \tag{7.14}$$

The operation of the Modified ICC is tabulated in Table 7.2 for various duty ratios. The output voltage increases as the duty ratio increases according to the Eqn. 7.13.

Table 7.2: Output Voltage according to Eqn. 7.13 for Modified ICC when the input voltage is V_g

Duty Ratio	Output Voltage	Types of Operation
0.1	-0.23 V_g	buck
0.2	-0.56V_g	buck
0.3	-1.04V_g	boost
0.4	-1.77V_g	boost

7.4 Calculation of Ripple Currents of Modified ICC

In practical realization of the Modified ICC, as shown in Fig.7.6, the circuit uses MOSFET switches, S_1 and S_2, high frequency ultrafast recovery diodes D_1 and D_2, are assumed to be ideal. But the inductors L_{1a}, L_{1b}, L_{2a} and L_{2b}, have their series resistances r_{1a}, r_{1b}, r_{2a} and r_{2b} respectively, while the capacitors C_1, C_2, C_{o1} and C_{o2} also have the equivalent resistances r_{c1},r_{c2}, r_{o1} and r_{o2}, shown in series, respectively. The average input voltage applied is V_g, the instantaneous input current flowing is denoted as i_g. Similarly, the average output voltage V_o is measured across a load resistance of R_L, and the instantaneous output current is denoted as i_o. The capacitors C_1 and C_2 act as primary means of storing and transferring energy from the input to the output. The average inductor voltages V_{L1a}, V_{L1b}, V_{L2a} and V_{L2b} are zero at steady state and are used effectively in formulating the output voltage equation by volt-second balance. The capacitors C_1 and C_2 are designed in such a way that it transfers energy from input to provide the constant voltage.

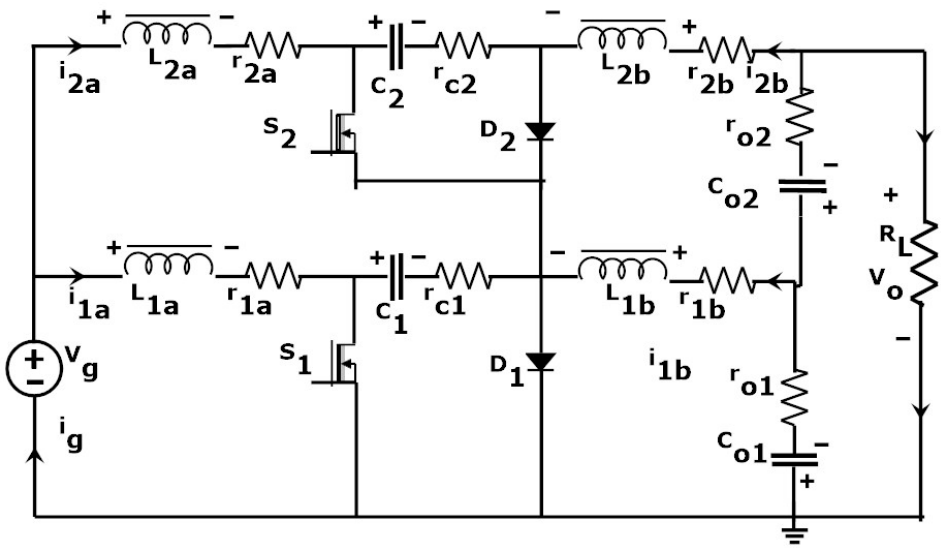


Fig. 7.6: Practical circuit diagram of Modified ICC

7.4.1 Mode 1 - S_1 ON and S_2 OFF (t_0 to t_1)

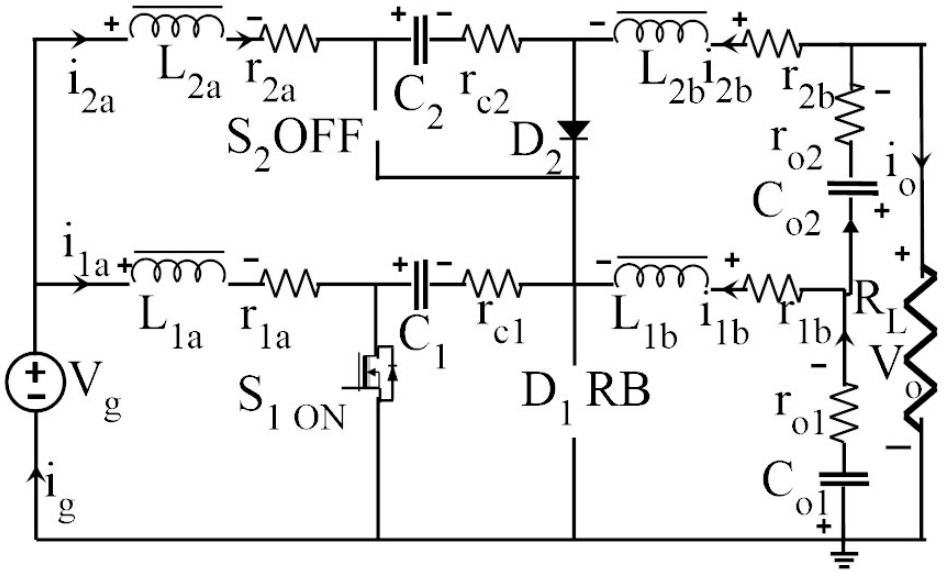


Fig. 7.7: The circuit diagram of Modified ICC when S_1 ON and S_2 OFF

The practical circuit diagram for the case when the switch when S_1 ON and S_2 OFF is shown in Fig.7.7. In this mode inductor L_{1a} is charging through the switch S_1. Also in the lower half of the circuit, the capacitor C_{o1} is charging and inductor L_{1b} is discharging and capacitor C_1 is discharging. The inductor L_{2a} is discharging and capacitor C_2 is charging through diode D_2, C_1 and switch S_1 to the ground. At the same time, the capacitor C_{o2} is discharging and inductor L_{2b} is charging, again through diode D_2, C_1 and also the switch S_1 to the ground. The PSPWM pulse sequence generated in Fig.7.2 triggers the MOSFET switches. The ripple current produced in the Modified ICC is derived to show that the ripple is much less

compared to the Proposed ICC. The Modified ICC produces less amount of ripple compared to that of CCC.

In Mode-1 when switch S_1 is turned ON as shown in Fig.7.7, the inductors L_{1a} is charged and L_{2a} is discharged simultaneously. The load current is assumed to be constant and flows in negative direction. The rise and fall of the inductor currents i_{1a} and i_{2a}, respectively are assumed to be linear. Now the ripple current on inductor L_{1a} and L_{2a} during Mode-1 is described by equations below

$$\Delta I_{L1a_{1ON}} = (t_1 - t_0)(V_g - r_{1a}i_{1a})/L_{1a} \tag{7.15}$$

$$\Delta I_{L2a_{1ON}} = \frac{(t_1 - t_0)}{L_{2a}} [V_g + V_{c1} - V_{c2} - r_{c1}(i_{1b} + i_{2b}) - (r_{2a} + r_{c1} + r_{c2})i_{2a}] \tag{7.16}$$

The ripple content on source current during Mode-1 is given by Eqn. (7.17), assuming $L_{1a} = L_{2a} = L_a$ also neglecting parasitic resistances,

$$\Delta I_{g_{1ON}} = \Delta I_{L2a_{1ON}} - \Delta I_{L1a_{1ON}} = (t_1 - t_0)(V_{c1} - V_{c2})/L_a \tag{7.17}$$

The ON time $t_1 - t_0$ is very low value (as duty ratio is always < 0.5) compared to that of CCC, hence the ripple current become very low. Also by controlling the inductor value ripple current can be reduced. The ripple content on load side by neglecting parasitic resistance values are given by equations (7.18) and (7.19)

$$\Delta I_{L1b_{1ON}} = (t_1 - t_0)(V_{c1} - V_{o1})/L_{1b} \tag{7.18}$$

$$\Delta I_{L2b_{1ON}} = (t_1 - t_0)(V_{c1} - V_{o1} - V_{o2})/L_{2b} \tag{7.19}$$

where $\Delta I_{L1a_{1ON}}, \Delta I_{L1b_{1ON}}, \Delta I_{L2a_{1ON}}$ and $\Delta I_{L2b_{1ON}}$ are ripple content on current I_{1a}, I_{1b}, I_{2a} and I_{2b} respectively.

7.4.2 Mode 2 - S_1 OFF and S_2 OFF (t_1 to t_2)

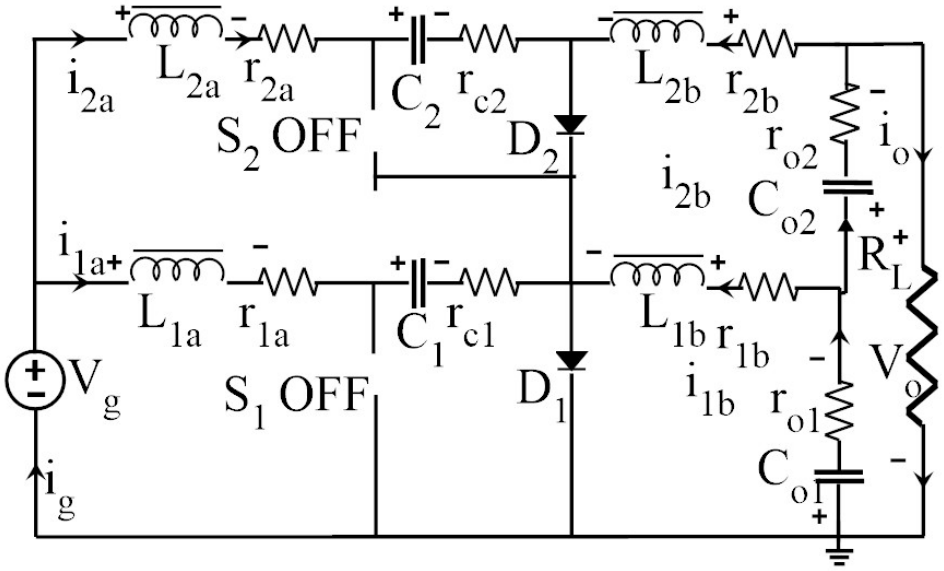


Fig. 7.8: The Circuit diagram of Modified ICC when S_1 and S_2 are OFF

The practical circuit diagram for the switches, when S_1 and S_2 OFF, is shown in Fig.7.8. In this mode, inductor L_{1a} and L_{2a} are discharging through the switch D_1 and D_2. Also the capacitor C_{o1} is discharging and inductor L_{1b} is charging and both the capacitors C_1 and C_2 are charging, through diodes D_2, D_1 to ground. The capacitor C_{o2} is charging and inductor L_{2b} is discharging through diodes D_2, D_1 connected to ground. Assuming inductor current to be falling linearly and neglecting parasitic resistances, the ripple current on source side is given by the equations (7.20), to (7.21)

$$\Delta I_{L1a_{1,2OFF}} = (t_2 - t_1)(V_g - V_{c1})/L_{1a} \tag{7.20}$$

$$\Delta I_{L2a_{1,2OFF}} = (t_2 - t_1)(V_g - V_{c2})/L_{2a} \tag{7.21}$$

The net ripple content on source current is given by the Eqn. (7.22).

$$\Delta I_{g_{1,2OFF}} = \Delta I_{L2a_{1,2OFF}} - \Delta I_{L1a_{1,2OFF}} = (t_2 - t_1)(-V_{c2} + V_{c1})/L_{2a} \tag{7.22}$$

Here again the ripple content source is very low since the duty ratio is always less than 0.5 and the OFF time $(t_2 - t_1)$ is very low. Further reduction in ripple content can be achieved by controlling the inductor values ripple content can be reduced. The ripple content on load side current is given by equations (7.23) and (7.24).

$$\Delta I_{L1b_{1,2OFF}} = -(t_2 - t_1)V_{o1}/L_{1b} \tag{7.23}$$

$$\Delta I_{L2b_{1,2OFF}} = -(t_2 - t_1)(V_{o1} + V_{o2})/L_{2b} \tag{7.24}$$

The ripple on load side can be controlled by the inductor values of L_{1b} and L_{2b}.

7.4.3 Mode 3 - S_1 OFF and S_2 ON (t_2 to t_3)

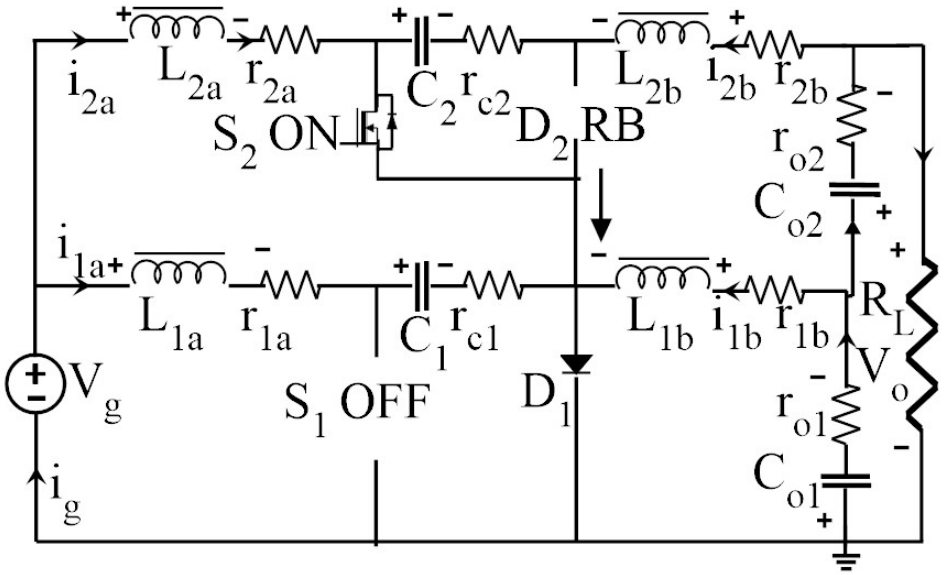


Fig. 7.9: The Circuit diagram of practical Modified ICC when S_1 OFF and S_2 ON (D_2 RB : Diode 2 Reverse Biased)

The effective circuit diagram for the switch when S_1 OFF and S_2 ON is shown in Fig.7.9. In this mode, the inductor L_{1a} is discharging and capacitor C_1 is charging through the diode D_1. Also inductor L_{1b} is charging to discharge the capacitor C_{o1}. At the same time, the inductor L_{2a} is charging through switch S_2 and diode D_1. The capacitor C_{o2} is charging, sending current through the inductor L_{2b} and the capacitor C_2 is discharging through diode D_1 to the ground. Assuming that the inductor currents i_{1a} and i_{2a} are assumed to be respectively falling and rising linearly, the ripple current, by neglecting

parasitic resistances, is given by equations (7.25), to (7.26)

$$\Delta I_{L1a_{2ON}} = (t_3 - t_2)(V_g - V_{c1})/L_{1a} \tag{7.25}$$

$$\Delta I_{L2a_{2ON}} = (t_3 - t_2)V_g/L_{2a} \tag{7.26}$$

The net ripple content on source current during Mode-3 is given by the Eqn. (7.27)

$$\Delta I_{g_{2ON}} = \Delta I_{L2a_{2ON}} - \Delta I_{L1a_{2ON}} = (t_3 - t_2)V_{c1}/L_{2a} \tag{7.27}$$

For the same case, the load side ripple current is given by the equations (7.28) and (7.29).

$$\Delta I_{L1b_{2ON}} = -(t_3 - t_2)V_{o1}/L_{1b} \tag{7.28}$$

$$\Delta I_{L2b_{2ON}} = (t_3 - t_2)(V_{c2} - V_{o1} - V_{o2})/L_{2b} \tag{7.29}$$

The ripple on output current can be controlled by varying ON time of switch S_2 and also with help of inductor values of L_{1b} and L_{2b}.

7.4.4 Mode 4 - S_1 and S_2 OFF (t_3 to t_4)

The effective circuit diagram for Mode-4 is same as that shown in Fig.7.8 and hence the switching behaviour is exactly similar to what was explained in Sec. 7.4.2 The expression for source and load ripple currents are also similar to what was given all Eqn. 7.20 to 7.24.

In all the expressions of the ripple current in Sec. 7.4.1 to 7.4.4, it may be noted that the ON times t_1 - t_0 and t_3 - t_2 and the OFF times t_2 -

t_1 and t_4 - t_3, are very small for the duty ratio of the Modified ICC, which is always < 0.5, as against that of CCC. This results in low value of switch current stress and ripple current. Also by controlling the inductor values in the expression for the source and load ripple, the ripple current can be further reduced. Accordingly the Modified ICC can promise to perform much better than the CCC

7.5 Design of Components

The components, $L_{1a}, L_{2a}, L_{1b}, L_{2b}, C_1, C_2, C_{o1}$ and C_{o2} of Modified ICC, described in Fig. 7.6 are designed [4] systematically for -40V, 80W output similar to Sec. 5.4. The design approach is very much similar to Sec. 5.4.2 and the Modified ICC is realized by adapting same components of ICC. The designed components for 80W output is tabulated in Table. 7.3.

Table 7.3: Design values for Modified ICC

parameter	Values	parameter	Values
V_g	20V	V_o	-40V
L_{1a}, L_{2a}	0.375 mH	L_{1b}, L_{2b}	0.75mH
C_1, C_2	10uF	C_{o1}, C_{o2}	10uF
R_L	20 Ω	f_s	25 kHz

7.6 Compensator Design - State Space Averaged Model of Modified ICC

In order to guarantee stable operation of the Modified ICC, it is imperative that control through the PSPWM pulse train is derived from the error that is fed back from the output voltage and the set voltage. The transfer function of the Modified ICC is therefore derived, further to asses the requirement of the compensation required in the feed back path. Towards this, the state space analysis [82] of the Modified ICC in all the four modes are carried out. For the state variable analysis, the state variables are defined below:
$i_{1a}(t)$- current through inductor L_{1a},
$i_{1b}(t)$- current through inductor L_{1lb},
$i_{2a}(t)$ - current through inductor L_{2a},
$i_{2b}(t)$- current through inductor L_{2b},
$v_{c1}(t)$- voltage across capacitor C_1,
$v_{c2}(t)$- voltage across output capacitor C_2,
$v_{o1}(t)$, voltage across capacitor C_{o1} and
$v_{o2}(t)$- voltage across output capacitor C_{o2}.
And the output variables are
$i_g(t)$- current through the source and
$v_o(t)$- voltage across load resistance.

The Modified ICC in continuous conduction mode can be modeled using state space averaging (SSA) technique as follows. The derivation of the state space model for all the four modes are summarized in Appendix C. The state matrices, to be included in the SSA model, are to be taken from the Appendix C in each of the modes are tabulated below.

The discussions in this section has lot of similarity to section 5.5, and hence only the subtle changes pertaining to the Modified ICC alone

Table 7.4: State matrices for four modes of operation of Modified ICC

Operation	**State Matrices**
Mode 1	A_1, B_1, C_1
Mode 2	A_2, B_2, C_2
Mode 3	A_3, B_3, C_3
Mode 4	A_4, B_4, C_4

are discussed here. The plant transfer function is given by Eqn. 7.30,

$$G_p(s) = \frac{\hat{v}^(s)}{\hat{d}(s)} = C_{m2}(sI - A)^{-1}((A_1 - A_2) + (A_3 - A_4))X \quad (7.30)$$

Where $\hat{v}(S)$ and $\hat{d}(S)$ are slight variations in the output voltage and duty cycle respectively, with respect to steady state values V_o and d the duty ratio. Also the variable C_{m2} is second row of output matrix, which is the equation for output voltage as described in Appendix C,

$$C_{m2} = d_1 * C_{mode1mR2} + d_1' * C_{mode2mR2} + d_2 * C_{mode3mR2} + d_2' * C_{mode4mR2} \quad (7.31)$$

The matrices A_1 - A_2 and A_3 - A_4 are evaluated from the components of the circuit as given below:

A_1 - A_2 =

$$\begin{bmatrix} \frac{r_{c1}}{L_{1a}} & 0 & 0 & 0 & \frac{1}{L_{1a}} & 0 & 0 & 0 \\ 0 & \frac{r_{c1}}{L_{1b}} & -\frac{r_{c1}}{L_{1b}} & -\frac{r_{c1}}{L_{1b}} & \frac{1}{L_{1b}} & 0 & 0 & 0 \\ 0 & -\frac{r_{c1}}{L_{2a}} & -\frac{r_{c1}}{L_{2a}} & -\frac{r_{c1}}{L_{2a}} & \frac{1}{L_{2a}} & 0 & 0 & 0 \\ 0 & -\frac{r_{c1}}{L_{2b}} & -\frac{r_{c1}}{L_{2b}} & -\frac{r_{c1}}{L_{2b}} & \frac{1}{L_{2b}} & 0 & 0 & 0 \\ -\frac{1}{C_1} & -\frac{1}{C_1} & -\frac{1}{C_1} & -\frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

A_3 - A_4 =

$$\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{r_{c2}}{L_{2a}} & 0 & 0 & \frac{1}{L_{2a}} & 0 & 0 \\ 0 & 0 & 0 & -\frac{r_{c2}}{L_{2b}} & 0 & \frac{1}{L_{2b}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_2} & -\frac{1}{C_2} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

The duty ratios of d_1 and d_2 can be varied upto 50%, to avoid overlap of turn ON of switches. The designed values of parameters for the Modified ICC, for experimental validation with FPGA controller, are mentioned in Table 7.3. The resulting s-domain

transfer function of the plant, in MATLAB R12a environment is obtained, after substituting the design values from Table (7.3) in the equation (7.30). Including the modulator gain, the transfer function is given below in equation (7.32).

$$G_p G_m(s) = \frac{(b_1 s^7 + b_2 s^6 + b_3 s^5 + b_4 s^4 + b_5 s^3 + b_6 s^2 + b_7 s + b_8)}{(s^8 + a_1 s^7 + a_2 s^6 + a_3 s^5 + a_4 s^4 + a_5 s^3 + a_6 s^2 + a_7 s + a_8)} \tag{7.32}$$

where $b_1 = 624.4, b_2 = 3.113 * 10^8, b_3 = -2.915 * 10^{11}, b_4 = 7.43 * 10^{16}$, $b_5 = -4.17 * 10^{19}, b_6 = 4.517 * 10^{24}, b_7 = 6.353 * 10^{25}, b_8 = 9.986 * 10^{30}$ $a_1 = 353.9, a_2 = 2.394 * 10^{08}, a_3 = 7.461 * 10^{10}, a_4 = 1.63 * 10^{16}, a_5 = 4.05 * 10^{18}, a_6 = 2.44 * 10^{23}, a_7 = 1.789 * 10^{25}, a_8 = 5.184 * 10^{29}$.

The bode plot of the equation 7.32 for plant as given in Fig. 7.10, shows a gain margin of -35.6 dB and phase margin of 7.35°.

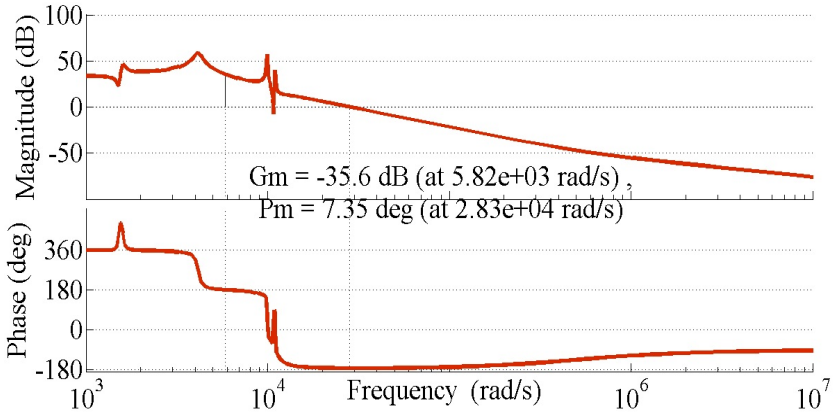


Fig. 7.10: Bode Plot of modified ICC without compensator.

So the system is obviously unstable. Including a type III compensator [80] with transfer function given Eqn. in the feed back path, brings out a phase margin of 52.5° and a gain margin 21.5dB, thus making the system stable.

$$G_c(s) = 300,000 * \frac{(s + 3952.2)^2}{s(s + 77490)^2} \tag{7.33}$$

And the overall transfer function in closed loop is

$$T(s) = \frac{Nr}{Dr} \tag{7.34}$$

where Nr= $1.873 * 10^8 s^9 + 9.487 * 10^{13} s^8 + 6.537 * 10^{17} s^7 + 2.306 * 10^{22} s^6 + 1.623 * 10^{26} s^5 + 1.604 * 10^{30} s^4 + 1.053 * 10^{34} s^3 + 2.431 * 10^{37} s^2 + 2.398 * 10^{40} s + 4.679 * 10^{43}$,
Dr = $s^{11} + 1.553 * 10^5 s^{10} + 6.299 * 10^9 s^9 + 3.93 * 10^{13} s^8 + 1.465 * 10^{18} s^7 + 2.978 * 10^{21} s^6 + 9.876 * 10^{25} s^5 + 6.216 * 10^{28} s^4 + 1.469 * 10^{33} s^3 + 1.878 * 10^{35} s^2 + 3.113 * 10^{39} s$

The bode plot of the overall compensated system of the transfer function in Eqn. 7.34 is shown in Fig. 7.11.

In order to complete the implementation, the s-domain transfer function of the compensator is converted to z-domain. The z-domain transfer function is implemented in the FPGA controller for practical realization of the Modified ICC. The z-domain transfer function of the compensator is given by the Eqn. 7.35.

$$G_c(z) = 10^{10} * \frac{(1.9509z^3 + 5.8526z^2 + 5.8526z + 1.9509)}{z^3 + z^2 - z - 1.0} \tag{7.35}$$

Towards this implementation, the digital compensator is modelled for the Eqn. 7.35 using XILINX tool in FPGA modulator.

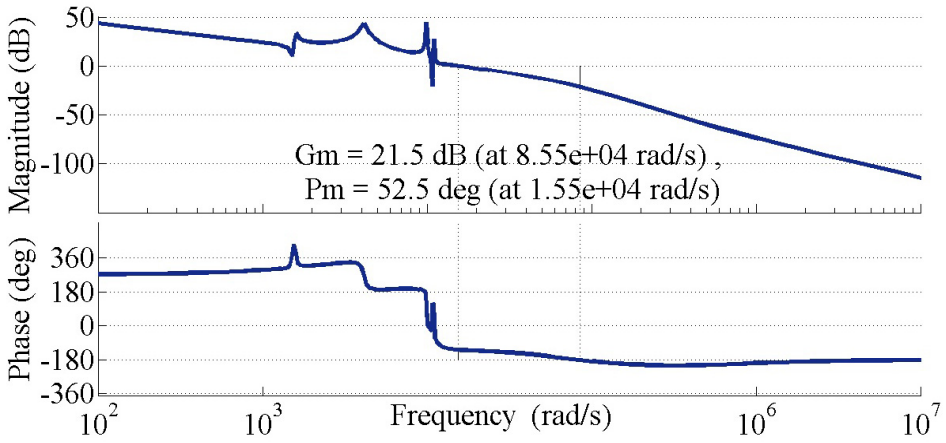


Fig. 7.11: Bode Plot of Modified ICC with compensator.

7.7 Simulation of Modified ICC

The Modified ICC, including the compensator, is simulated in closed loop with designed values as shown in Table 7.3. The parasitic resistance values of inductors and capacitors are included, during the simulation of the converter in closed loop. As shown in Fig. 7.12, the output voltage is compared in an error detector with set value of -40V. The error is processed in compensator, whose output is compared with carrier signal at 25KHZ to produce the PSPWM trigger switches. These Phase shifted PWM pulse train is used to turn ON the switches of the Modified ICC as shown in Fig.7.3. The performance of the circuit in simulation, assessed in terms of input and output voltage, input and output current and transient response, is discussed in the sections to follow:

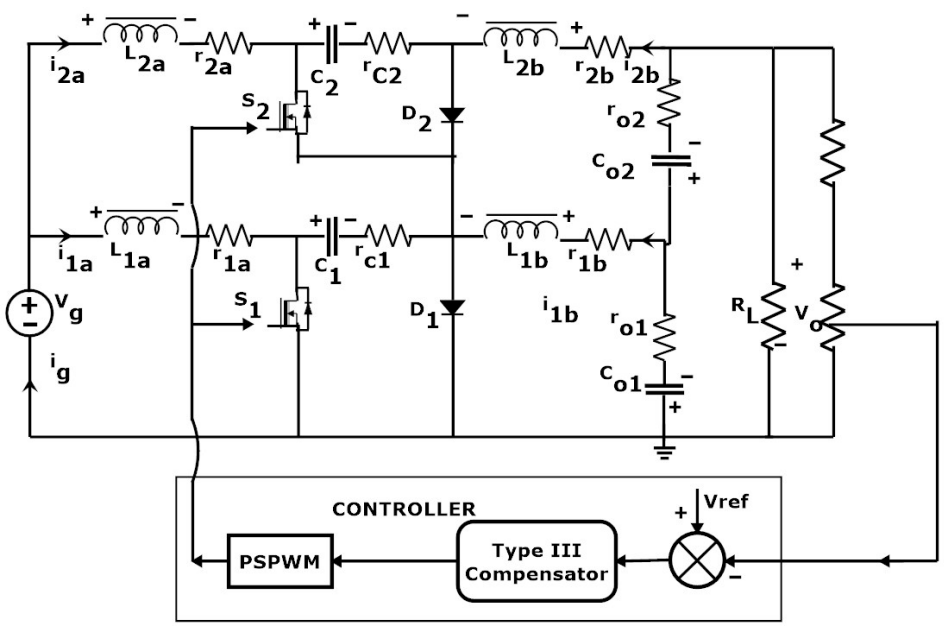


Fig. 7.12: Block diagram of Modified ICC in closed loop for simulation

7.7.1 Voltage

The output voltage shown in Fig. 7.13 is plotted against time. The duty ratio evaluated for -40V output from equation 7.13 is $d_1 = d_2$ = d =0.43. The interleaved output voltages V_{o1} and V_{o2} are 15V and 25V respectively in closed loop against the duty ratio $d = 0.43$. The expected value of -40V at the output for an input voltage of 20V, is seen to be produced in Fig. 7.13, as Vo = -40V. The output is seen to settle within 20ms, with nil overshoot. This may be contrasted with the settling time of the ICC [9], which is 400 ms. The settling time can further be reduced by decreasing output inductor values. As is clear from the plot of the output in Fig. 7.13, the output voltage is

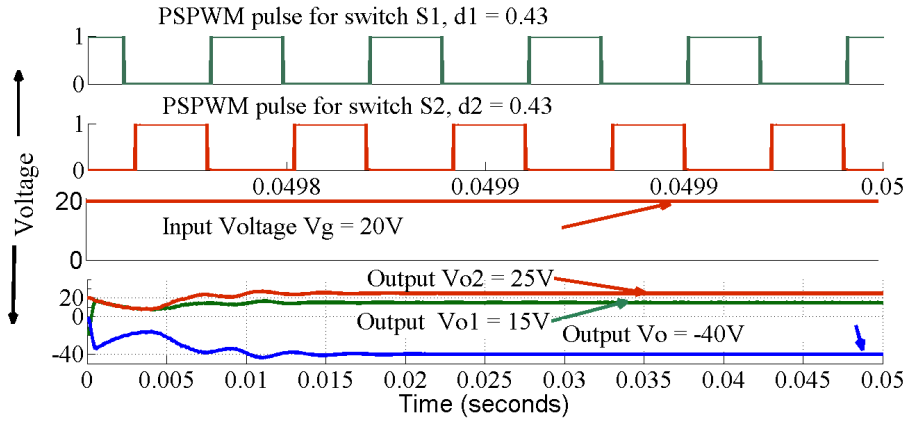


Fig. 7.13: The output voltage of Modified ICC, PSPWM duty ratio 0.43, input voltage V_g =20V, Interleaved voltages V_{o1} =15V, V_{o2} =25V, Output voltage, V_o = -40V. The PSPWM sequence is also shown for clarity

sum of two interleaved voltages and with the value greater than input voltage, the boosting has been achieved for a duty ratio of 0.43. The interleaved output voltages are having different magnitudes according the eqquations 7.7 and 7.11. The reduction in switching stress during the boost operation is an additional advantage.

7.7.2 Current

The source and inductor current waveforms plotted against time in Fig.7.14. The extent of reduction of ripple in the output is commendable, coming to less than 1 %. The ripple in input current ripple has also come down considerably compared to the earlier design discussed, viz. the CCC and the Proposed ICC, as shown in the Fig.7.14. The ripple on source current is 200mA, only 4.4 % of source current, though the ripple for inductor current is 410mA.

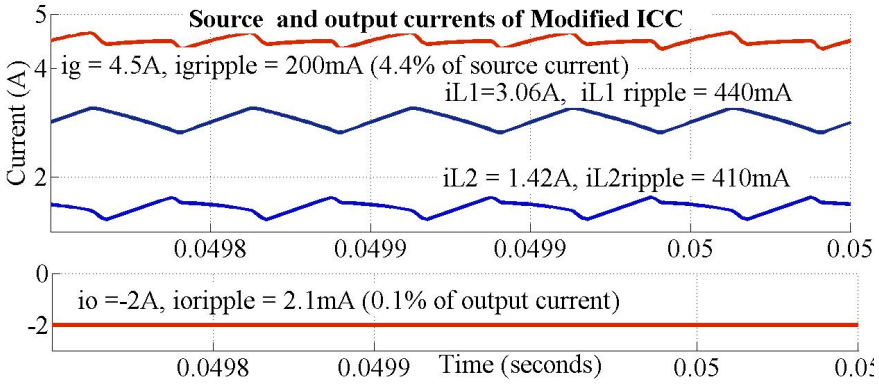


Fig. 7.14: Drawing a Source current $I_g = 4.5$A, the Modified ICC produces an output Current I_o = -2A. Inductor currents $I_{a2} = 3.1$A, $I_{a1} = 1.4$A and sum upto I_g

The switch current of switch S_1 is shown in Fig. 7.15. The switch current is measured at an input voltage of 20V and output of -40V,-2A, using a current measurement block connected in series with the MOSFET. Though the peak value of switch current is measured as 7.7A, the relatively less time taken for the switch to be kept on, thanks to the duty ratio of 0.43 less than 0.5, brings down the switching stress. The switch current of switch S_2 is shown in Fig. 7.16 measures as 5.1A.

The peak value of switch current is measured as 5.1A. The switch current of S_2 is lower than that of S_1, because the switch S_1 has to carry the total current during Mode -1. But switch S_2 has to carry only its branch current during Mode - 3. So while selecting the switch rating S_2 can be selected to carry low value of current.

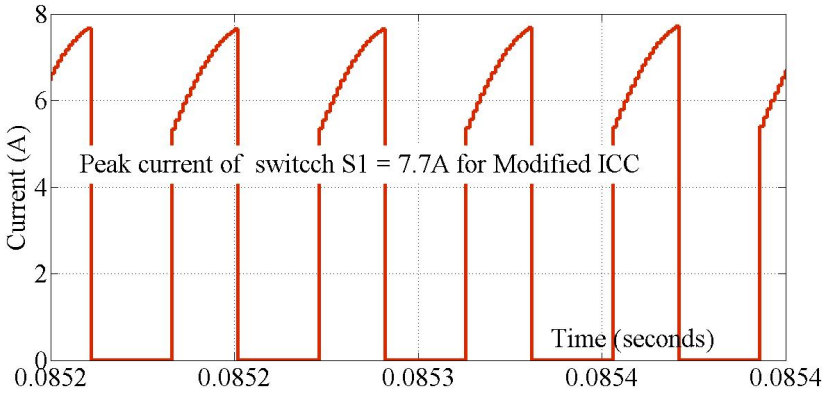


Fig. 7.15: Switch current of switch S_1. Peak value of switch current =7.7A.

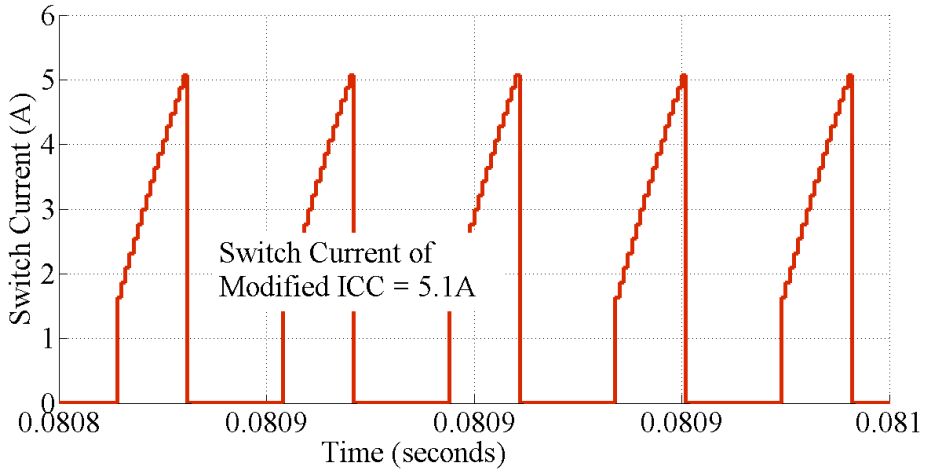


Fig. 7.16: Switch current of switch S_2. Peak value =5.1A.

7.7.3 Transients

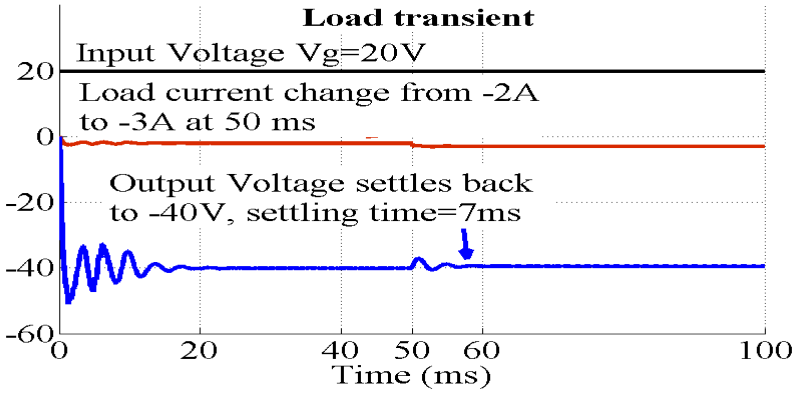


Fig. 7.17: Load transient for constant -40V output , for load current changes from -2A to -3A.

A noticeable trait of the Modified ICC is fast settlement during transients. The transient waveform for a load current change from -2A to -3A is shown in Fig. 7.17. To achieve this test condition, for an input voltage 20V is applied, load current is changed from -2A to -3A. It can be seen that the output voltage -40V settles back within 10ms, after the change. The transient of the load current is shared in two interleaved circuits by the inductors L_{1b} and L_{2b}, hence the overshoot and settling time are reduced.

7.8 Summary

The present chapter has demonstrated the design and simulated testing in MATLAB of a Modified ICC, which has proposed a

modification in the circuit topology of the ICC. A note worthy feature of the design is that the Modified ICC, provides multiple output voltage with duty ratio less than 0.5. The multiple outputs correspond to both boost and buck modes of operation. As against the Conventional Cuk / Interleaved Cuk Converter reported in literature, the Modified ICC converter also provides a boost output with the low duty ratio below 0.5, while the others in comparison provides only buck operation with duty ratio below 0.5. Also all three output voltages form the Modified ICC can be varied directly from the duty ratio. The admirably small ripple in both the input and the output current underscores the merit of the design proposed here. The reduction in the switching stress while achieving the boost operation is a major boon in the design. The quick recovery of the output voltage from transient changes holds out the promise of the Modified ICC in effectively handling sudden changes in load, as in the case of welding and electric vehicles.

Chapter 8

Practical Validation of Modified Interleaved Cuk Converter

8.1 Introduction

The findings of theoretical and simulation analysis of Modified ICC is further strengthened by experimental validation through hardware realization, presented in the present Chapter. Closed loop control of Modified ICC is demonstrated in this chapter by realizing the Modified ICC as an electronic circuit, with hardware components like switches, diodes, inductor and capacitors. The feed back path including compensator and error detector are appended to the circuit using the XILINX Spartan - 3AN FPGA Altium Nano board with level shifting circuit. The circuit diagram for closed loop control is shown in Fig. 8.1. The circuit realized has the following specifications:

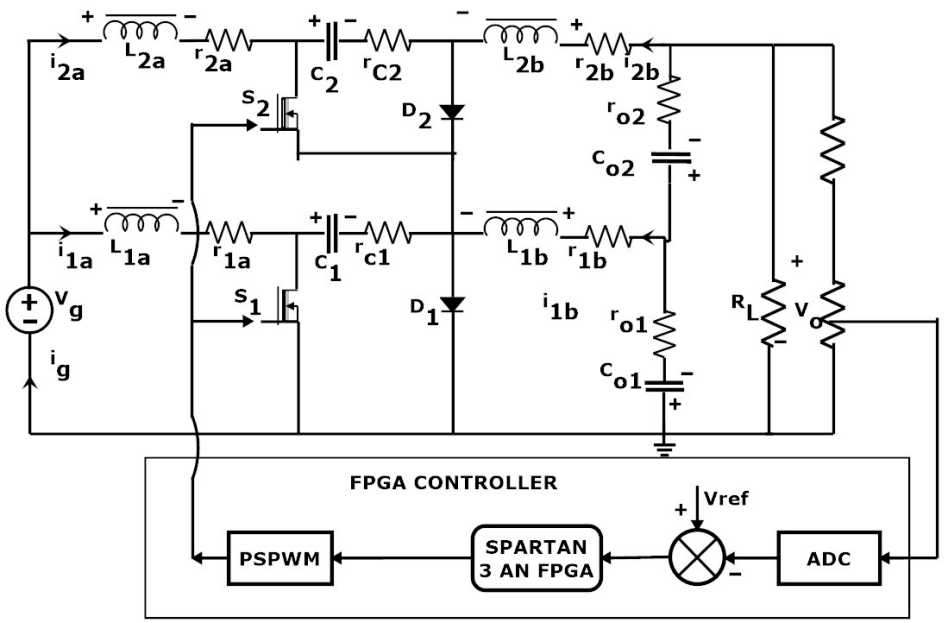


Fig. 8.1: Circuit for closed loop control of Modified ICC in hardware

1. Input voltage : 20 V
2. Output voltage : -40 V
3. Interleaved voltages V_{o1} = 14 V and V_{o2} = 26V
4. Duty ratio $d_1 = d_2 = \mathrm{d} = 0.42$
5. Carrier frequency : 25 kHz.
6. Load current : 2 A
7. The power circuit board is constructed for 100W, due to limitations in laboratory set-up.

The inductors and capacitors are selected for 100W output in the Modified ICC, as explained in section 6.2. While the capacitors of 10μF, MOSFETs IRF540 and diodes of MUR 810, MUR 420 are chosen from available stock, the inductors are designed and wound on an E-55 ferrite core. Twenty nine turns of three conductors of 22 SWG wire in parallel are wound on E-55 core to obtain $L_{1a} = L_{2a} =$ 0.38mH and $L_{1b} = L_{2b} = 0.75$mH is obtained by winding 42 turns of a SWG 20 wire on E-55 core.

A 30V, 5A DC source is used to provide 20V input to power circuit board. The separate 5V, DC source supplies the auxiliary supply for current sensor board while a 12V source powers the TLP-250 opto coupler circuits, used for switching S_1 and S_2. In the Modified ICC circuit the switches (S_1, S_2) are at different potentials at source terminal and also S_2 is not connected to ground. So the TLP250 opto coupler circuits are used here for isolation and switching.

A 100Ω, 5A variable rheostat is used as load, to set the current required during testing. While ammeters and voltmeters are used for the measurements of input and output current and voltages, a LA-55P current sensor board is used to monitor the waveforms of input, output and inductor currents. A 50MHz, 2 channel and 100MHz, 4 channel DSOs complete the test set up.

The photograph of the resulting lay out of the realization is shown in Fig. 8.2. The hardware realized for Modified ICC is tested extensively for output voltage and current, ripple content in the input and output voltages and current, the switching currents and the transient response of the circuit. The sections to follow summarizes the results as seen on the oscillograms. The efficiency of the circuit realized is also measured and presented.

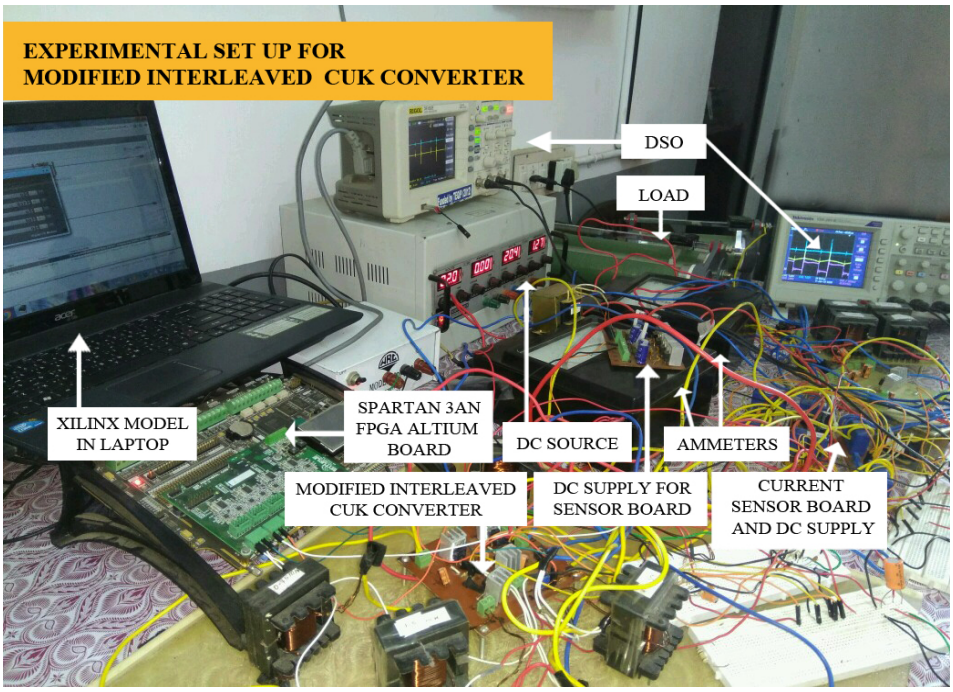


Fig. 8.2: Photograph: Experimental set up of Modified ICC PCB along with XILINX FPGA controller board

8.2 Results and Discussions

The phase shifted PWM waveform used for realizing the Modified ICC in closed loop for a duty cycle of 0.4, is shown in Fig. 8.3. The duty ratio of PWM pulse required to produce same output (-40V) in CCC is distributed into two PWM signals in PSPWM. It has observed that both the pulses are judiciously phase shifted in time, so that there exists a common OFF time as shown in Fig.8.3. It is interesting to note that that the duty ratio of PWM for Modified ICC is reduced to half of that for CCC, which can bring down the switching stress

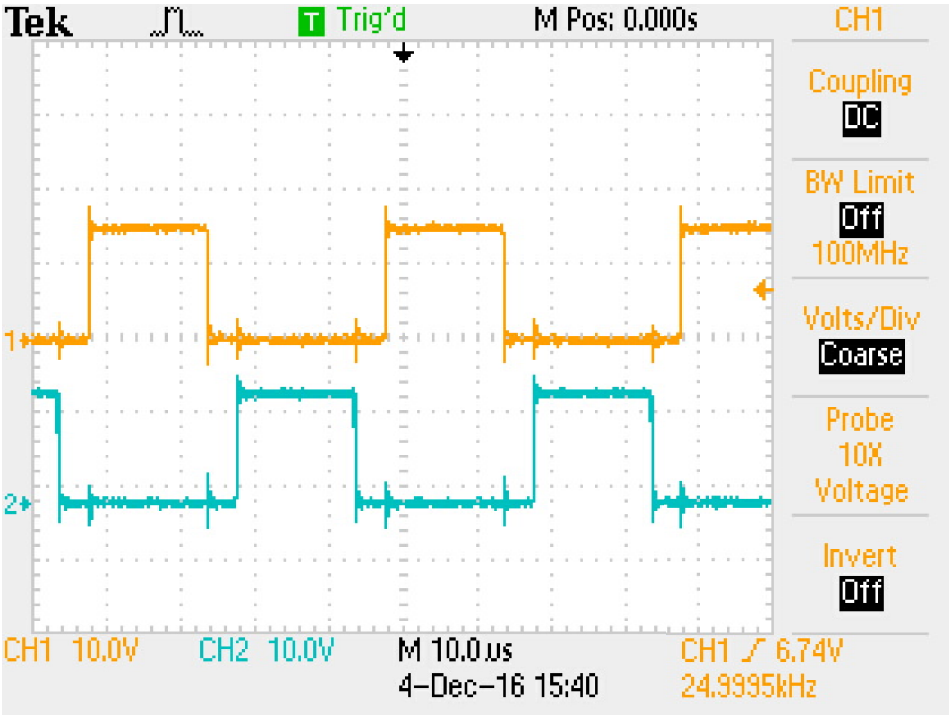


Fig. 8.3: PSPWM in closed loop for Modified ICC $d_1 = d_2$ =0.42

considerably.

8.2.1 Voltage

The PSPWM waveform with input voltage and output voltage is shown in Fig. 8.4. Corresponding to the PSPWM waveform for the duty ratio 0.43, the input voltage 20V (in pink, CH3) and output voltage -40V (in green, CH4) are shown in Fig. 8.4. The channels 1 and 2 (CH1 and CH2) provides PSPWM of duty ratio d=0.43, which

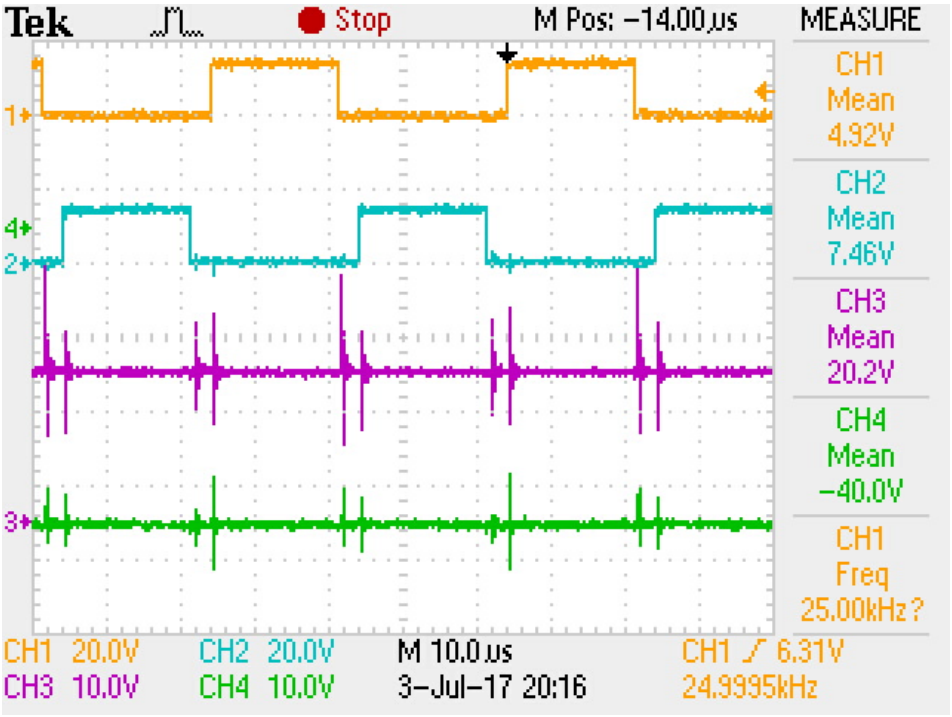


Fig. 8.4: CH1, CH2- PSPWM with $d_1 = d_2 = 0.43$, CH3- $V_g = 20V$, CH4- Output voltage $V_o = -40V, V_{orip} = -1.08V$ 2.7% of V_o

are applied two switches of the two legs of Modified ICC. The spikes appearing on the waveforms are due to the pick up on the sensing probes. Measurement on a finer scale confirms a ripple of -1.08 V (i.e. 2.7%) on the output voltage of -40V.

The interleaved output voltages, responsible for producing the output voltage of -40 V, for the duty ratio of d=0.43 are shown in Fig. 8.5a and 8.5b.

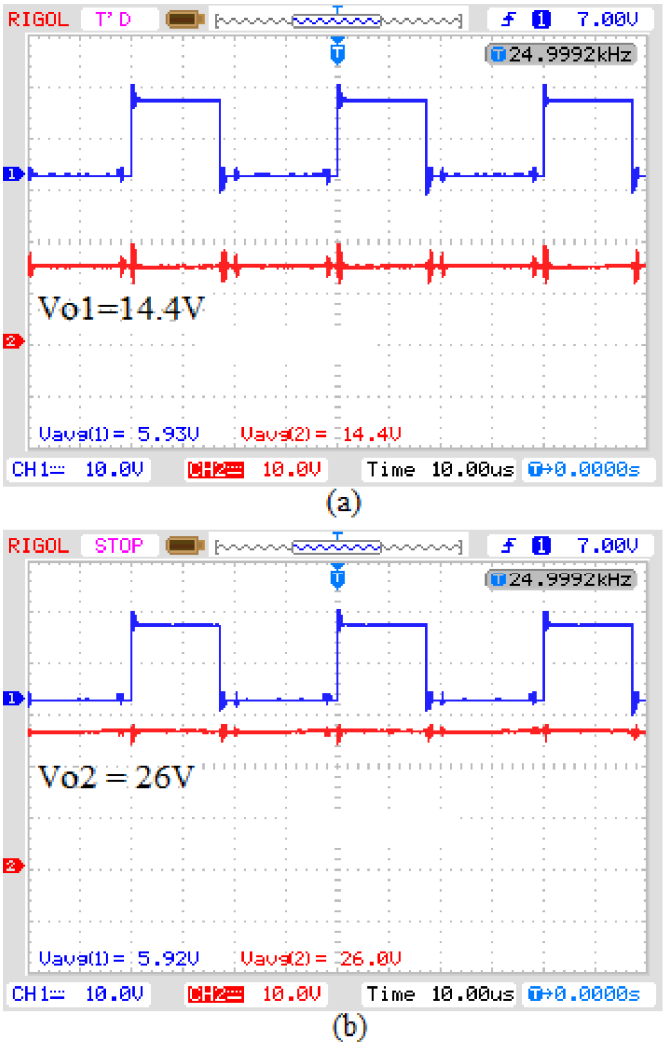


Fig. 8.5: Interleaved voltages V_{o1}=14.4V and V_{o2}=26V for duty ratio d =0.43 in closed loop

The interleaved voltage V_{o1} (Fig. 8.5a) measured as 14V and V_{o2} (Fig. 8.5b) as 26V for the duty ratio 0.43 are seen to satisfy the equations (7.7) and (7.11) respectively. For a slightly lower duty ratio of d=0.4, the Fig.8.6 shows the output voltage (interleaved voltage V_{o1} = 13V, (in red, CH2) as confirmed by Eqn. (7.7) The influence of the

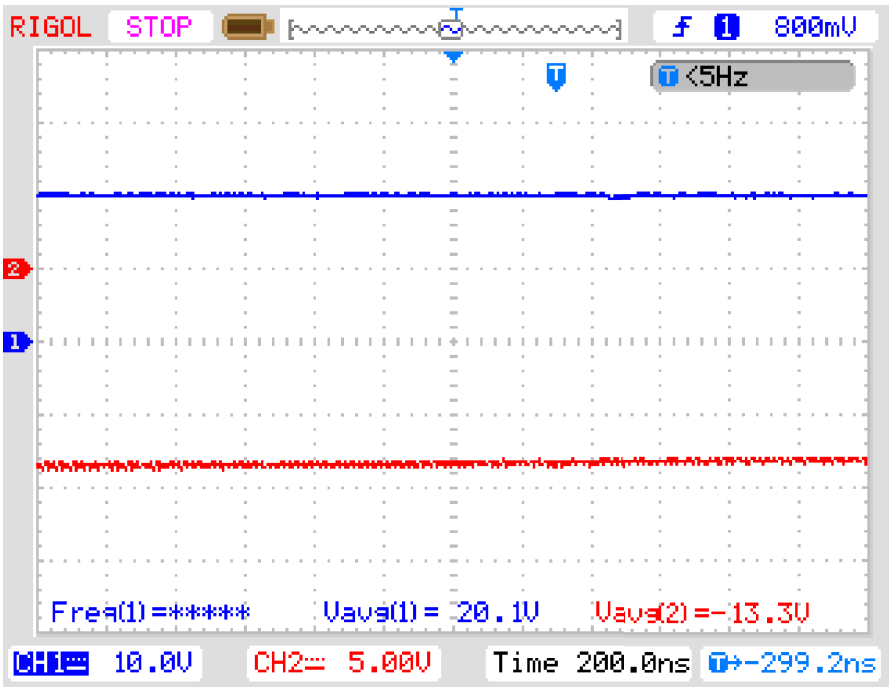


Fig. 8.6: The interleaved Output voltage V_{o1} of Modified ICC in closed loop

interleaved voltages on the duty cycle as indicated in the Eqn. (7.7) is underscored by the above observation.

8.2.2 Current

The input and output currents of Modified ICC measured from the hardware realization are shown in Fig. 8.7. The ripple on source

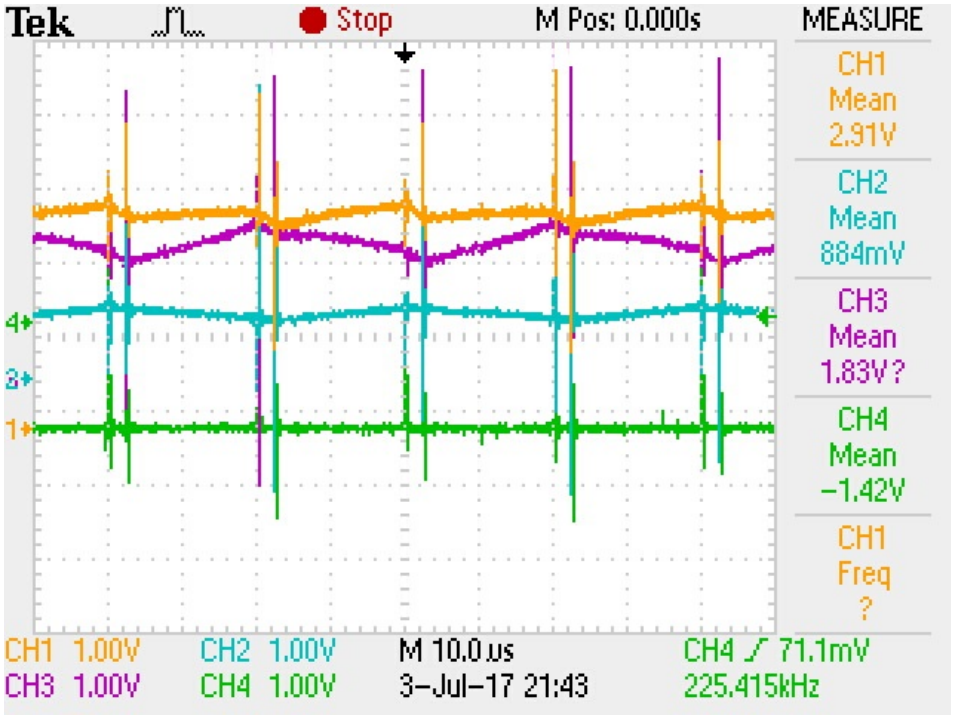


Fig. 8.7: CH1-Source current $I_g = 2.91A$, $I_{g_{rip}} = 200mA$ (7% of I_g), CH2-inductor current $I_{1a} = 0.88A$, CH3-inductor current $I_{2a} = 1.83A$, CH4-output current $I_o = -1.42A$,$I_{o_{rip}} = 75mA$ (5.37% of I_o) of Modified ICC in closed loop

current is 200mA for an input current of 2.9A, limiting the percentage of ripple to only 7% of source current. The ripple on load current is 75mA for a load current of 1.83A, showing the ripple in percentage as

only 5.4%. The appreciable reduction of the ripple content in Modified ICC is quite palpable, in contrast to that of CCC.

The waveforms corresponding to the switching current of switch S_1 is portrayed in Fig.8.8., along with PSPWM corresponding to duty ratio 0.43 in channel 1 (CH1 amber). The channel 2 (CH2 green) shows the

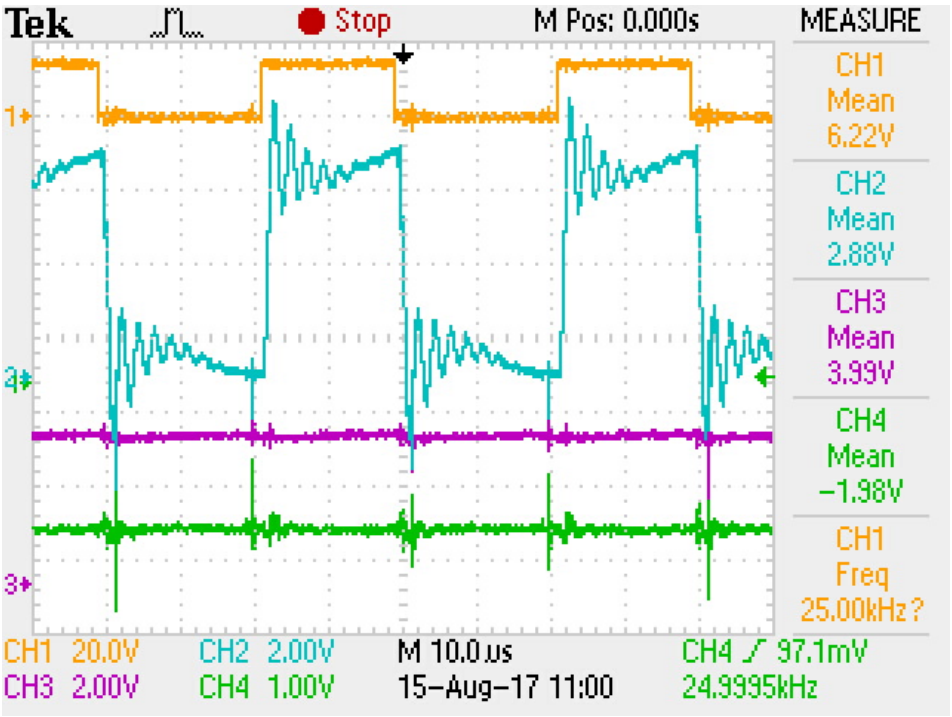


Fig. 8.8: Switch current of S_1 of Modified ICC in closed loop (current sensor scaled as 1V= 1A): CH1-PSPWM duty ratio d=0.43, CH2-switch (S_1) current, peak value =7A, CH3-source current $I_g = 3.99A$, CH4-output current $I_o = -1.98A$

switch current of S_1, indicating that the peak value of switch current is 7A, corresponding to 3.99A of input current I_g , shown in channel 3

(CH3 pink). The channel 4 (CH4 dark green) shown the load current is measured at this instance as -1.98A . It can be seen that the switch current is 1.75 times the input current and also 3.5 times the load current.

Fig. 8.9 illustrates the switch current of S_2. The channel 1 (CH1)

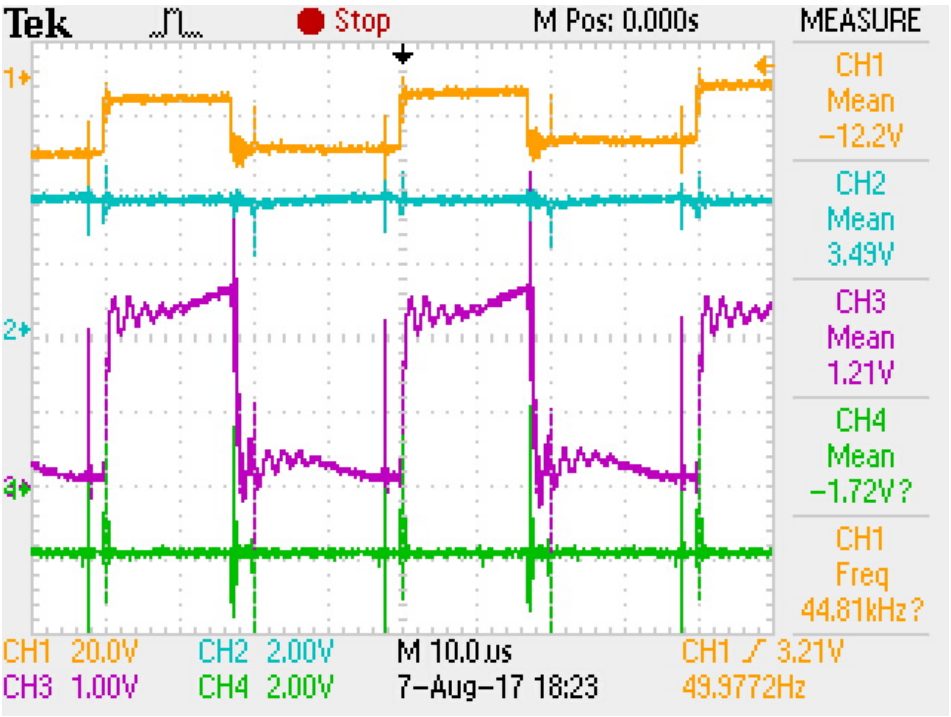


Fig. 8.9: Switch current of S_2 of Modified ICC in closed loop (current sensor scaled as 1V= 1A): CH1-PSPWM pulse d = 0.43, CH2-source current I_g=3.5A, CH3-Switch S_2 current, peak value =5.0A , CH4-I_o = $-1.72A$

shows PSPWM corresponds to duty ratio 0.43, Channel 2 (CH2) shows the input current of 3.49A, peak value of switch S_2 current is 5A

corresponds to -1.72A output current as in channel 4 (CH4). The switch current in S_2 is only 2.9 times the load current.

8.2.3 Transient

The transient behaviour of the hardware realized for the Modified ICC in response to change in load current is shown in Fig.8.6. When the

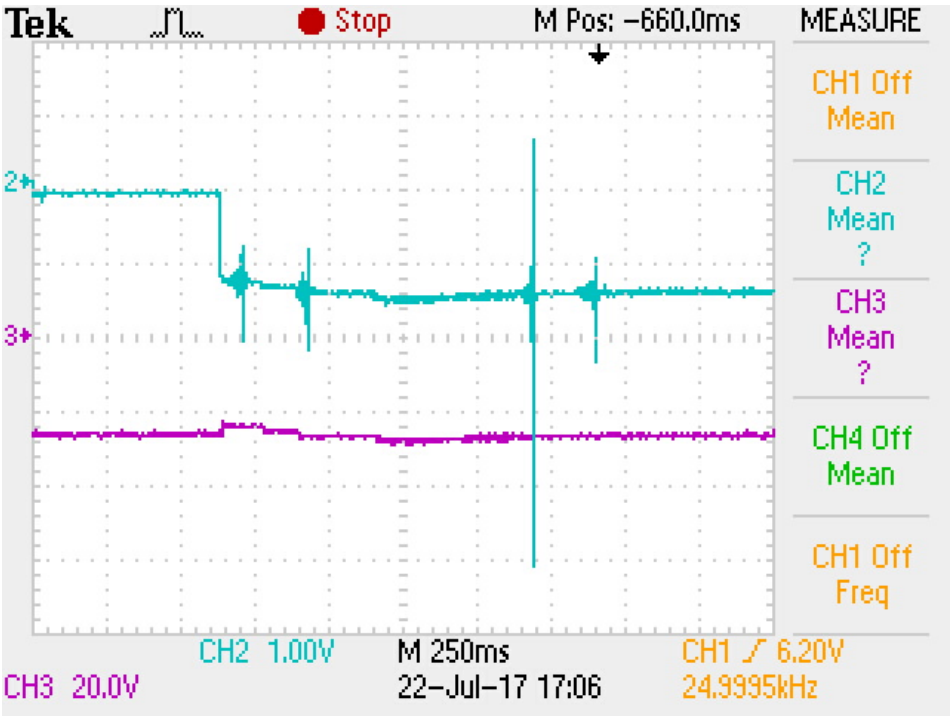


Fig. 8.10: Load transient of Modified ICC : Corresponding to a change from - 0.4A to -1.4 A of load current, while delivering -24V the output voltage quickly settles back to -24V.

converter is running with a small load of 0.4A and delivering 24V output from a 20V input, the load current is changed from 0.4A to 1.4A. It can be seen that the output voltage settles back to 24V after a transient in less than 250 ms. The quick recovery in response to the load change of the Modified ICC will be an attractive feature in electric cars, where large changes are likely very frequently.

8.2.4 Efficiency

In order to asses the efficiency of the converter, the input voltage is kept constant at 20V and the load current is varied from no load to -2A, the output voltage and input current are measured respectively with voltmeter and ammeter.

The 100Ω rheostat is varied to change the load current, the output voltage is driven to a constant value by the designed type III compensator. The measurements are simultaneously observed in DSO, ammeters, voltmeters and multimeter.

The measurements are tabulated in Table 8.1. It can be seen that the output voltage is almost constant, providing a very tight regulation. It is also interesting to note that the variation of the input current is almost linear with load current. The efficiency is evaluated by taking ratio of the load power to input power for a constant line voltage. As a result, the converter provides an efficiency above 90%, which is more or less constant over the change of load.

The corresponding efficiency curve of the Modified ICC is shown in Fig. 8.11. It can be seen that the efficiency is lowest at light load, while the efficiency increases as the loading moves towards the rated load conditions.

Table 8.1: Efficiency of Modified ICC converter at $f_s = 25kHz$

V_g (V)	I_g (A)	P_i (W)	V_o (V)	I_o (A)	P_o (W)	Efficiency (%)
20.1	1.04	20.9	-40.1	-0.47	18.4	90.2
20.1	1.13	22.7	-40.1	-0.515	20.7	90.9
20	1.85	37	-40.0	-0.859	34.5	92.8
20	2.33	46.6	-39.8	-1.08	43	92.2
20	2.91	58.2	-39.7	-1.38	54.8	94.1
19.9	3.53	70.3	-39.3	-1.67	65.6	93.4
20.1	4.1	82.4	-38.9	-1.97	76.7	92.9

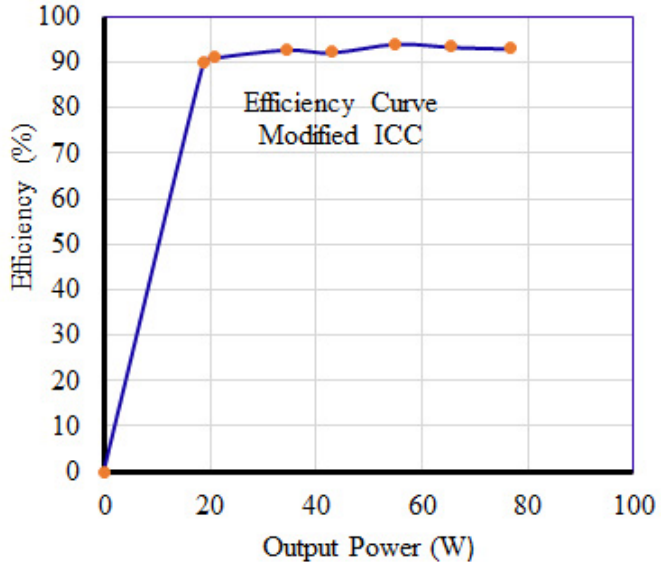


Fig. 8.11: Efficiency curve of Modified ICC in the hardware realization

The measurements corresponding the vital observables of the design in the hardware validation of the Modified ICC are tabulated in Table

8.2. The measurements are compared with those from the hardware

Table 8.2: Results for Modified ICC $f_s = 25kHz$,d=0.43

Parameter	Experimental Results
V_g	20v
V_o for d=0.5	-60V
I_{grip}	200mA for 2.9A (7% of I_g)
I_{orip}	75mA (5.3%)
V_{orip}	1.08V (2.7%)
$I_{1switch}$ at -40V	7.2A
$I_{2switch}$ at -40V	5.6A
Load Transient	300ms
Efficiency	93%

realization of CCC in Table 8.3. A substantial reduction in all the observables along with an enhanced efficiency underscores the merit of the Modified ICC.

Table 8.3: Comparison of CCC and Modified ICC - Hardware at V_g = 20 V, V_o = -40 V, I_o = -2 A, f_s = 25 kHz

Parameter	CCC	Modified iCC
$I_{g(rip)}$	800 mA (17.3%)	200 mA (6.8%)
$V_{o(rip)}$	1.5 V(3.8%)	1.08 V (2.7%)
$I_{o(rip)}$	100 mA (5%)	75 mA (3.7%)
Load transient	400 ms	250 mS
Efficiency (average)	89%	93%

8.3 Summary

The hardware realization of the Modified ICC reposted in this chapter brings out the correspondence with the theoretical models proposed earlier in Chapter 7 and also the simulation experiments carried thereon. It is seen that the boost operation has been made possible with the duty ratio of the PWM reduced to half what was required for the CCC. The converter provides three output voltages (of which two are boosted outputs) with variable magnitudes, where the variation is possible directly with duty ratio. The attractive features of the design as has been brought out through the hardware realization include low ripple content in the input and output currents, reduced switching currents, tight regulation over large variation in load and above all an appreciably high efficiency more than 90%, which is more or less flat over a large variation of load current. The capability of the Modified ICC to recover fast from transient changes in the loading currents adds to the versatility of the design. The findings of this chapter in comparison with Proposed ICC and CCC are communicated to standard journal for publication. A comparison with the CCC in respect of the features listed above finally speaks loud of the merits of the design proposed.

Chapter 9

Conclusions and Directions for Further Research

9.1 Consolidation of Results

In an attempt to arrive at the proper topology for a guaranteed performance, the thesis has portrayed the systematic evolution of three types of DC to DC Converters viz. the Conventional Cuk Converter (CCC), the proposed Interleaved Cuk Converter (Proposed ICC) and the Modified Interleaved CuK converter (Modified ICC). The detail design based on the theoretical propositions followed by detailed simulation, supplemented by hardware realization has directed the process to assess the improvement in the performance of the DC to DC Converter, as the thesis evolved. This chapter comprises the results of CCC, Proposed ICC and Modified ICC, consolidated through detailed hardware realization. The results obtained from the hardware of all three

converters reveal the practical aspects, strengthening the observations made in the present thesis.

9.2 Comparison of Salient Features

While CCC produces only one output voltage, the Proposed ICC provides two parallel output voltages. Both the circuits primarily operate with a duty ratio less than 0.5 and results into a buck opeation. Any attempt to operate these two circuits in boost mode demands duty ratio more than 0.5, resulting in increased switching stress in both the circuits and ripple building issues in Proposed ICC. On the other hand, the major development from the thesis the Modified ICC has been shown to operate with duty ratio less than 0.5 and concurrently produce three output voltages, with different magnitudes - two are interleaved outputs and third is the sum of interleaved two outputs. The resulting sum obviously produces boost output, at the same time maintaining the duty ratio less than 0.5, thereby alleviating the evils of enhanced switching stress and ripple building. The large number of output voltages make the Modified ICC more versatile for applications. All converters are noted for having output voltages with opposite polarity to input voltage.

9.2.1 Number of Output Voltages and Influence of Duty Ratio

CCC is shown to produce -20V output for a duty ratio of 0.5 with 20V input, while lower voltages as possible with duty ratio less than 0.5. However, for a boost operation of the CCC, duty ratios more than 0.5 are required, which can lead to enhanced switched stress . The

proposed ICC produces same output (-20V) for the same duty ratio with the same input 20V. Modified ICC produces -60V for a duty ratio of 0.5 with the same input of 20V and the output voltage is three times the input voltage.

9.2.2 Ripples on Current and Voltage

The source current ripple at -15V output voltage for CCC is 400 mA which is 27% (of source current). But for the same output voltage the Proposed ICC produces only 100 mA ripple and it is only 5.5% of source current. The reduction in ripple has been achieved because of the cancellation taken place during the paralleling of the interleaved outputs. However for a boost operation of CCC to produce -40V, the source current ripple is 800mA which is 17.3% (of source current). The requirement of duty ratio greater than 0.5 has also resulted in higher ripple content, in addition to enhanced stress already noted. Interestingly the Modified ICC for the same output voltage of -40V produces 200 mA ripple and is only 6.8% of source current. Apparently larger value of ripple current in comparison to the Proposed ICC could be attributed to the modified circuit topology introduced to realize the boost operation. It can be seen that the Modified circuit forces the output current to flow through diode D_1. For the same reason the interleaved voltages also take different values as confirmed by the Eqn. (7.13) even when operated with same duty ratio $d_1 = d_2$. The output voltage of CCC has 1.04V ripple which is 7%, when operated for an output voltage of -15V. But for the same output the ripple of Proposed ICC appreciably comes down to 400mV which is 2.7%. However, the output voltage of CCC has 1.4V ripple, which is 4%, when operated for an output voltage of -40V. For the same output of -40V the Modified ICC produces a ripple of 1.08V, which is 2.7% as against the CCC.

9.2.3 Peak Switch Current

The switch current peak value of CCC at -15V, -2A output is 6.5A whcih is 3.25 times the load current; but for the same output voltage and current the switch peak current is 2 times the load current for the Proposed ICC, clearly bringing out the benefit of interleaved operation. At the output of -40V, -2A, the switch peak current of CCC is 9.5A i.e. 4.5 times the load current, which is objectionably high. But that for Modified ICC for the same output voltage and current an effective distribution of switching currents to both the halves brings down the current to 7.2A for S_1 and 5.6A for S_2. The appreciable reduction to 3.6 and 2.8 times the load current, respectively underscores the merit of the Modified ICC.

9.2.4 Efficiency

The average efficiency of the three configurations over a variation of 2A of load current is tabulated in Table 9.1. It can be seen that the Modified ICC gives the best efficiency both in the buck and boost operations. At -40V, -2A output, the CCC offers an efficiency of 89%, which may be contrasted with the efficiency of 94% for the Modified ICC. The Proposed ICC is seen to provide an efficiency of 91% at -15V, -4A. The reduction in the ripple resulting from the interleaved operation accounts for the higher efficiency.

9.2.5 Output Voltage vs Duty Ratio

The graph showing the relationship between duty ratio and the output voltage is plotted in Fig. 9.1. The input voltage to the converter is 20V for all three types of converters shown on the graph.

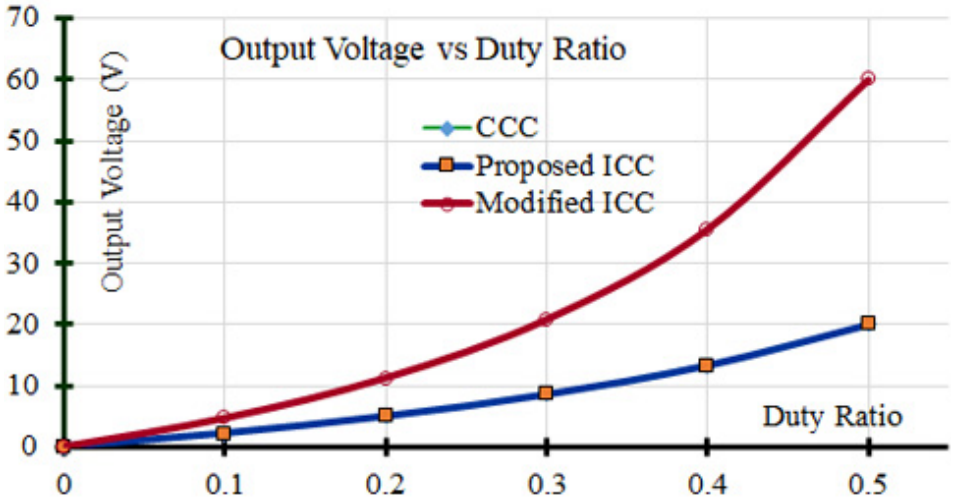


Fig. 9.1: Plot of Output Voltage vs Duty ratio for the circuits of CCC, Proposed ICC and Modified ICC with input voltage $V_g = 20V$

It can be seen that the CCC and ICC provide less than 100% output voltage, at a duty ratio not greater than or equal to 0.5. Also the curves of these two converters coincide each other, since they have same output voltage equation. The above two converters can perform boost operation only by increasing the duty ratio above 0.5, which in turn can cause for high switching stress in CCC and ripple building issues in the Proposed ICC. On the other hand, the Modified ICC totally overcome this problem and it provides up to 300% output, even when the duty ratio is limited to 0.5 .

The consolidation of performance, discussed thus far for the hard ware realized for CCC, Proposed ICC and Modified ICC is tabulated in Table 9.1.

Table 9.1: Consolidation of results of hardware realization of CCC, Proposed ICC and Modified ICC

Parameter	CCC	Proposed ICC	Modified ICC
No.of O/P Voltages	1	2 parallel	3 different
Output Voltage with d= 0.5	-20V	-20V	-60V
$I_{g(rip)}$ at -15V (% of I_g)	400mA (27%)	100mA (5.5%)	–
$I_{g(rip)}$ at -40V (% of I_g)	800mA (17.3%)	–	200mA (6.8%)
$V_{o(rip)}$ at -15V	1.04V (7%)	400mV (2.7%)	-
$V_{o(rip)}$ at (-40V)	1.5V (3.8%)	-	1.08 V (2.7%)
Load transient	400 mS	250 mS	250 mS
Switch Current peak (at -15V)	6.5A (3.2 times)	4A (2 times)	–
Switch Current peak (at -40V) (multiples of I_o)	9.5A (4.5 times)	-	7.2A (3.6 times for S_1), 2.9 times for S_2
Efficiency	89%	91%	94%

9.3 Final Conclusions of the Thesis

In an attempt to evolve a DC to DC converter with multiple outputs and high efficiency, the thesis has reported the design, development, simulation and the hardware realization of the Modified ICC. The idea of the Modified ICCC has been built up systematically after studying the existing designs in detail. The limitations of the Conventional Cuk

Converter (CCC) in offering both the buck and the boost operations, with the well sought out traits of DC to DC Converter like low ripple, high efficiency, quick transient response and low switching stress were demonstrated convincingly in the initial chapters. The work reported here further moved on to modify the Interleaved Cuk Converter, with a modification in the switching process, with the possible improvement in reducing the switching stress, thanks to the interleaved topology.

The Proposed ICC, as it is named in the thesis, was demonstrated to bring down the switching stress, improve the efficiency and reduce the ripple content. But the boost output from Proposed ICC creates ripple building issues and it wipes out the merits of interleaved topology. Also the possibility of getting multiple outputs from a single DC to DC converter put still could not be achieved. It is in this context, the Modified ICC proved to offer multiple outputs with buck and boost voltages, at the same time providing tangible improvement in performance in respect of desired features also.

The comparison of the salient features achieved in the design and development of the three converters, as elaborated in Sec. 9.2, brings out the outcome of the new topology viz. the Modified ICC, proposed in the thesis. The performance figures, as consolidated after detailed simulation and a systematic hardware realization has helped to add credence to the work reported in this thesis.

The major findings of the thesis also have been reported in standard publications and they are either in print or in the review stage, as summarized in the list of publications that have evolved from the thesis. A systematically built hardware as part of the experimental demonstration of the ideas put forward in the present thesis substantiates the findings, thereby adding credence to the work reported.

9.4 Directions for Future Work

It is accepted that the ICC topology gives better performance compared to all present available known techniques. The possibility of controlling the output voltage and the resulting ripples in the load current, directly using the duty ratio could be boon in prototyping the design. The closed loop control of the converter can be modified by current programmed control method so that the transformer saturation in isolated converters can be eliminated. This topology can be extended to Bidirectional Converters to cater the requirements in renewable energy applications. An attractive option would be to explore the possibility of using resonant switching of the topology proposed in the thesis, so as to reduce the switching losses and improve the efficiency. Working further on the hard ware realized, the reduction of the size of the inductors could be achieved using coupled inductors and the ripple can be further steered. Thus the converter can me made compact, which can help in embedded applications. Another phase of ICC could be added to further reduce ripple of the source. The work reported in the present thesis can be extended directly to AC side to assess the THD and power factor. Some efforts extend the work in direction is progressing now as a direct spin off form the thesis, and some preliminary results have been published in journal.

The requirement to provide multiple outputs from a DC to DC converter, with a high efficiency and tight regulation is essential in laboratories, Electric vehicles, personal computers, digital TVs, medical equipments and a host of other applications, which now depend on electric power. With variety of unconventional power sources dominating in the energy market, DC to DC converters, with multiple outputs, are becoming a well justified demand of the industry.

In those applications which require high currents, the size of the energy storage elements could be a very large and the interleaving helps to reduce the size of the individual components and the stress on the switching devices. With the advent of host of alternatives power sources like solar cells and fuel cells, and development in the battery technology offering large energy density, the demand for DC to DC converters with a tight regulation and high efficiency will be on increase. It is interesting to note that there is an increasing trend use DC for welding, especially for precision welding. The transient response of the Modified ICC could prove to be a good candidate to handle the sudden changes in current, required during welding.

The thesis has throws open further avenues in improving the regulation and efficiency, even when the output impedance of the primary source is varying drastically over leading conditions. The effective solution then would be to estimate the source impendence on line and accommodate the changes in the design of the compensator. The possibility of using machine learning techniques to effectively learn the source parameters to be included in the design of the duty ratio is worth exploring. But the fact that the possibility getting multiple outputs from a single DC to DC converter, supplemented with all the good qualities of a power supply will be the base line that can strengthen further research in the development of DC to DC converters.

List of Publications, come out of thesis

Journals

- Joseph K.D., Asha Elizabeth Daniel, A. Unnikrishnan, "Interleaved cuk converter with improved transient performance and reduced current ripple," IET Journal of Engg., Vol. 2017, Issue.7, 2017, pp. 362-369, doi:10.1049/joe.2017.0153, ESCI,Clarivate Analytics.
- Joseph K.D., Asha Elizabeth Daniel, A. Unnikrishnan, "Improvement of Power Factor by Input Filter and Ripple Reduction using Cuk Converter in Continuous Conduction Mode," International Journal of Engineering and Advanced Technology., Vol. 8, Issue.6, 2019, pp. 4938-4945, doi: 10.35940/ijeat.F9244.088619, Elsevier, Scopus.

Conferences

- Joseph K.D., Asha Elizabeth Daniel and A. Unnikrishnan, "Reduced ripple interleaved cuk converter with phase shifted PWM," Proc. IEEE 10^{th} Asian Control Conf., Kota, Malaysia, Jun. 2015, pp. 1-6, doi: 10.1109/ ASCC.2015. 7244782.
- Joseph. K.D., Asha Elizabeth Daniel, A. Unnikrishnan, "Interleaved Cuk Converter with Reduced Switch Current," Proc. IEEE, 5^{th} Biennial International Conference on Power, Instrumentation, Control and Computing (PICC),Thrissur, India, 18-20 Jan. 2018, pp 1-6, doi:10.1109/ PICC. 2018. 8384803.

Papers communicated and under Review

- Joseph K..D., Asha Elizabeth Daniel and A. Unnikrishnan, "Power Quality Analysis of Interleaved Cuk Converter with Rectifier and LCL filter, " IET Journal of Engineering, Clarivate Analytics. Communicated on 20.07.2019.
- Joseph K.D., Asha Elizabeth Daniel and A. Unnikrishnan, "Output Voltage Improvement by Modified Interleaved Cuk Converter with Low Duty Ratio, " Arabian Journal of Science and Engineering, SCIE. Communicated on 08.01.2020.

Bibliography

[1] R. G. Bedford, B. D.; Hoft, *Principles of Inverter Circuits. New York*. Newyork: John Wiley & Sons, Inc. ISBN 0-471-06134-4., 1964.

[2] I. P. R. Mallory & Co., ed., *Fundamental Principals of Vibrator Power Supply Design*. Indianapolis: P. R. Mallory & Co., Inc., first ed. ed., 1947.

[3] Y.-f. Liu, E. Meyer, and X. Liu, "Recent Developments in Digital Control Strategies for DC / DC Switching Power Converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 11, pp. 2567–2577, 2009.

[4] D. W. Hart, "DC-DC Converters," in *Power Electronics*, ch. 6, pp. 226–230, India: McGraw Hill Education (India) Private Ltd., 8 ed., 2011.

[5] L. COSEL CO., "AC-DC, DC-DC Converter Manufacturers," 2019.

[6] S. Cuk, "A new zero-ripple switching DC-to-DC converter and integrated magnetics," *IEEE Transactions on Magnetics*, vol. 19, no. 2, pp. 57–75, 1983.

[7] K. M. Smedley and S. Cuk, "Dynamics of One-Cycle Controlled Cuk Converters," *IEEE Transactions on Power Electronics*, vol. 10, no. 6, pp. 634–639, 1995.

[8] G. Umanand, L, Ranganathan, "Power factor improvement using," *IEE Proceedings Electric Power system Applications*, vol. 146, no. 2, pp. 231–236, 1999.

[9] Y. Gu and D. Zhang, "Interleaved boost converter with ripple cancellation network," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 3860–3869, 2013.

[10] H. Yan, S. Chen, Q.-m. Luo, and L.-w. Zhou, "Interleaved high step-up zero-voltage-switching boost converter with variable inductor control," *IET Power Electronics*, vol. 7, no. 12, pp. 3083–3089, 2014.

[11] A. A. A. Freitas, F. L. Tofoli, E. M. Sá Junior, S. Daher, and F. L. M. Antunes, "Analysis of high voltage step-up nonisolated DCDC boost converters," *International Journal of Electronics, Taylor & Francis*, vol. 103, no. 5, pp. 898–912, 2016.

[12] K. H. Chao and Y. C. Jheng, "A soft-switching coupled inductor bidirectional DCDC converter with high-conversion ratio," *International Journal of Electronics, Taylor & Francis*, vol. 105, no. 1, pp. 164–190, 2018.

[13] J. C. Rosas-Caro, F. Mancilla-David, J. C. Mayo-Maldonado, J. M. Gonzalez-Lopez, H. L. Torres-Espinosa, and J. E. Valdez-Resendiz, "A Transformer-less High-Gain Boost Converter With Input Current Ripple Cancelation at a Selectable Duty Cycle,"

IEEE Transactions on Industrial Electronics, vol. 60, no. 10, pp. 4492–4499, 2013.

[14] M. Ciobotaru, V. G. Agelidis, M. Jang, and H. Choi, "Performance evaluation of interleaved high-gain converter configurations," *IET Power Electronics*, vol. 9, no. 9, pp. 1852–1861, 2016.

[15] M. Muhammad, M. Armstrong, and M. Elgendy, "A Non-isolated Interleaved Boost Converter for High Voltage Gain Applications.," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 352–362, 2015.

[16] Y. F. Wang, L. K. Xue, C. S. Wang, P. Wang, and W. Li, "Interleaved High-Conversion-Ratio Bidirectional DC-DC Converter for Distributed Energy-Storage Systems-Circuit Generation, Analysis, and Design," *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5547–5561, 2016.

[17] X. He, C. Xu, W. Li, Y. Gu, H. Yu, and X. H. Wuhua Li, Chi Xu, Hongbing Yu, Yunjie Gu, "Analysis, design and implementation of isolated bidirectional converter with winding-cross-coupled inductors for high step-up and high step-down conversion system," *IET Power Electronics*, vol. 7, no. 1, pp. 67–77, 2014.

[18] M. Jang, H. Choi, and V. G. Agelidis, "Zero-current-switching bidirectional interleaved switched-capacitor DCDC converter: analysis, design and implementation," *IET Power Electronics*, vol. 9, no. 5, pp. 1074–1082, 2016.

[19] B. Akhlaghi and H. Farzanehfard, "Family of ZVT interleaved converters with low number of components," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 11, pp. 8565–8573, 2018.

[20] J. H. Yi, W. Choi, and B. H. Cho, "Zero-Voltage-Transition Interleaved Boost Converter with an Auxiliary Coupled Inductor," *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 5917–5930, 2017.

[21] J. Ebrahimi, S. H. Hosseini, E. Babaei, and T. Nouri, "Interleaved high step-up DCDC converter based on three-winding high-frequency coupled inductor and voltage multiplier cell," *IET Power Electronics*, vol. 8, no. 2, pp. 175–189, 2015.

[22] R. T. H. Li and C. N. M. Ho, "An active snubber cell for N-phase interleaved dc-dc converters," in *International Power Electronics and Application Conference and Exposition*, pp. 953–958, IEEE, 2014.

[23] R. T. H. Li and C. N. M. Ho, "An Active Snubber Cell for N-Phase Interleaved DC-DC Converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 344–351, 2016.

[24] S. Chen, L.-w. Zhou, Q.-m. Luo, and B.-x. Zhu, "Interleaved non-isolated high step-up DC/DC converter based on the diodecapacitor multiplier," *IET Power Electronics*, vol. 7, no. 2, pp. 390–397, 2014.

[25] R. Hosoki and H. Koizumi, "High-step-up dc-dc converter using voltage multiplier cell with ripple free input current," in *IECON Proceedings (Industrial Electronics Conference)*, no. 1, pp. 834–839, IEEE, 2013.

[26] V. A. K. Prabhala, P. Fajri, V. S. P. Gouribhatla, B. P. Baddipadiga, and M. Ferdowsi, "A DC-DC Converter with High Voltage Gain and Two Input Boost Stages," *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4206–4215, 2016.

[27] Y. Lu, Y. Xing, and H. Wu, "A PWM Plus Phase-Shift Controlled Interleaved Isolated Boost Converter Based on Semiactive Quadrupler Rectifier for High Step-Up Applications," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 7, pp. 4211–4221, 2016.

[28] L. Zhang, D. Xu, G. Shen, M. Chen, A. Ioinovici, and X. Wu, "A high step-up DC to DC converter under alternating phase shift control for fuel cell power system," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1694–1703, 2015.

[29] K. Tseng and C.Huang, "High Step-up High Efficiency Interleaved Converter With Voltage Multiplier Module for Renewable Energy System," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 3, pp. 1311–1319, 2014.

[30] S. J. F. Y. Hu, R. Zeng, W. Cao, J. Zhang, "Design of a Modular, High Step-Up Ratio DCDC Converter for HVDC Applications Integrating Offshore Wind Power," *IEEE Transactions on Industrial Electronics*, vol. 69, no. 4, pp. 2190–2202, 2016.

[31] Y. Hu, J. Wu, W. Cao, W. Xiao, P. Li, S. J. Finney, and Y. Li, "Ultrahigh Step-up DC-DC Converter for Distributed Generation by Three Degrees of Freedom (3DoF) Approach," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4930–4941, 2016.

[32] Y. Huangfu, S. Zhuo, F. Chen, S. Pang, D. Zhao, and F. Gao, "Robust Voltage Control of Floating Interleaved Boost Converter for Fuel Cell Systems," *IEEE Transactions on Industry Applications*, vol. 54, no. 1, pp. 665–674, 2018.

[33] A. Khosroshahi, M. Abapour, and M. Sabahi, "Reliability evaluation of conventional and interleaved DC-DC boost

converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5821–5828, 2015.

[34] F. Marvi, H. Farzanehfard, and E. Adib, "Zero voltage switching interleaved coupled inductor synchronous buck converter operating at boundary condition," *IET Power Electronics*, vol. 9, no. 1, pp. 126–131, 2016.

[35] I.-o. Lee, S.-y. Cho, and G.-w. Moon, "Interleaved Buck Converter having low switching losses and improved step-down conversion ratio," in *8th International Conference on Power Electronics - ECCE Asia*, pp. 2136–2143, 2011.

[36] I.-o. Lee, S.-y. Cho, and G.-w. Moon, "Interleaved Buck Converter Having Low Switching Losses and Improved Step-Down Conversion Ratio," *EEE Transactions on Power Electronics*, vol. 27, no. 8, pp. 3664–3675, 2012.

[37] J. M. Wang and S. T. Wu, "A Synchronous Buck DC-DC Converter Using a Novel Dual-Mode Control Scheme to Improve Efficiency," *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 6983–6993, 2017.

[38] O. Kirshenboim and M. M. Peretz, "High-Efficiency Nonisolated Converter with Very High Step-Down Conversion Ratio," *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 3683–3690, 2017.

[39] C. Chang, Y. Yuan, T. Jiang, and Z. Zhou, "Field programmable gate array implementation of a single-input fuzzy proportional-integral-derivative controller for DC-DC buck converters," *IET Power Electronics*, vol. 9, no. 6, pp. 1259–1266, 2016.

[40] P. Deivasundari, G. Uma, C. Vincent, and K. Murali, "Non-linear intermittent instabilities and their control in an interleaved DC

/ DC converter," *IET Power Electronics*, vol. 7, no. 5, pp. 1235–1245, 2014.

[41] B. Lin, C. Chao, and B. Hou, "Implementation of an interleaved three-level PWM converter with ZVS/ZCS functions," in *10th International Conference on Power Electronics and Drive Systems (PEDS)*, pp. 580–585, IEEE, 2013.

[42] B.-r. Lin and C.-c. Chen, "Analysis , Design and Implementation of an Interleaved DC / DC Converter with Series-Connected Transformers," *International Journal of Electronics, Taylor & Francis*, vol. 103, no. 2, pp. 322–341, 2016.

[43] C. F. Chuang, C. T. Pan, and H. C. Cheng, "A novel transformerless interleaved four-phase step-down DC converter with low switch voltage stress and automatic uniform current-sharing characteristics," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 406–417, 2016.

[44] K. I. Hwu, W. Z. Jiang, and P. Y. Wu, "An Expandable Four-Phase Interleaved High Step-Down Converter with Low Switch Voltage Stress and Automatic Uniform Current Sharing," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 10, pp. 6064–6072, 2016.

[45] E. Adib, B. Poorali, M. Esteki, and H. Farzanehfard, "High step-down interleaved buck converter with low voltage stress," *IET Power Electronics*, vol. 8, no. 12, pp. 2352–2360, 2015.

[46] W. Huang and J. A. Abu Qahouq, "Input Voltage Ripple-Based Sensorless Current Sharing Autotuning Controller for Multiphase DC-DC Converters," in *Applied Power Electronics Conference and Exposition (APEC)*, pp. 622–627, IEEE, 2015.

[47] W. Huang and J. A. Abu Qahouq, "Input Voltage Ripple-Based Sensorless Current Sharing Autotuning Controller for Multiphase DC-DC Converters," *IEEE Transactions on Industry Applications*, vol. 52, no. 5, pp. 4117–4125, 2016.

[48] M. Esteki, E. Adib, H. Farzanehfard, and S. A. Arshadi, "Auxiliary circuit for zero-voltage-transition interleaved pulse-width modulation buck converter," *IET Power Electronics*, vol. 9, no. 3, pp. 568–575, 2016.

[49] H. Wu, K. Sun, L. Zhu, and Y. Xing, "An Interleaved Half-Bridge Three-Port Converter With Enhanced Power Transfer Capability Using Three-Leg Rectifier for Renewable Energy Applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 606–616, 2016.

[50] N. A. Ahmed and J. Y. Madouh, "High-frequency full-bridge isolated DCDC converter for fuel cell power generation systems," *Springer Electrical Engineering*, vol. 100, no. 1, pp. 239–251, 2018.

[51] W. Huang and B. Lehman, "Analysis and Verification of Inductor Coupling Effect in Interleaved Multiphase DC-DC Converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 5004–5017, 2016.

[52] W. Huang and B. Lehman, "A Compact Coupled Inductor for Interleaved Multiphase DC-DC Converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 6770–6775, 2016.

[53] G. Calderon-Lopez, A. J. Forsyth, and D. Wu, "Discontinuous conduction/current mode analysis of dual interleaved buck and boost converters with interphase transformer," *IET Power Electronics*, vol. 9, no. 1, pp. 31–41, 2016.

[54] P. D. Antoszczuk, R. G. Retegui, N. Wassinger, S. Maestri, M. Funes, and M. Benedetti, "Characterization of Steady-State Current Ripple in Interleaved Power Converters Under Inductance Mismatches," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1840–1849, 2014.

[55] M. R. Banaei and B. H. A. Faeghi, "A Novel Structure for Single-Switch Nonisolated Transformerless BuckBoost DCDC Converter," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 1, pp. 198–205, 2017.

[56] Y. Zheng, M. Ho, J. Guo, and K.-l. Mak, "A Single-Inductor Multiple-Output Auto-Buck-Boost DC DC Converter With Autophase Allocation," *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 2296–2313, 2016.

[57] X. Huang, F. C. Lee, Q. Li, and W. Du, "High-Frequency High-Efficiency GaN-Based Interleaved CRM Bidirectional Buck / Boost Converter with Inverse Coupled Inductor," *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4343–4352, 2016.

[58] H.-K. Liao, T.-J. Liang, L.-S. Yang, and J.-F. Chen, "Non-inverting buckboost converter with interleaved technique for fuel-cell system," *IET Power Electronics*, vol. 5, no. 8, p. 1379, 2012.

[59] H. Wu, T. Mu, H. Ge, and Y. Xing, "Full-Range Soft-Switching-Isolated Buck-Boost Converters with Integrated Interleaved Boost Converter and Phase-Shifted Control," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 987–999, 2016.

[60] N. Mohammadian and M. R. Yazdani, "Half-bridge flyback converter with lossless passive snubber and interleaved technique," *IET Power Electronics*, vol. 11, no. 2, pp. 239–245, 2018.

[61] V. Senthilkumar, D. Parvathyshankar, and A. Thangavelu, "Zero voltage switching-pulse width modulation technique-based interleaved flyback converter for remote power solutions," *IET Power Electronics*, vol. 9, no. 7, pp. 1381–1390, 2016.

[62] S.-w. Lee and H.-l. Do, "Zero-Ripple Input-Current High-Step-Up Boost SEPIC DC DC Converter With Reduced Switch-voltage Stress," *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 6170–6177, 2017.

[63] H. Zhang, C. Yi, and T. Wei, "Non-linear modal analysis of transient interaction behaviours in SEPIC DC DC converters," *IET Power Electronics*, vol. 10, no. 10, pp. 1190–1199, 2017.

[64] B.-r. Lin, P.-l. Chen, and J.-j. Chen, "Interleaved Sepic Converter with Low Switching Loss," in *TENCON - IEEE Region 10 Conference*, pp. 1817–1822, IEEE, 2010.

[65] S. K. Haghighian, S. Tohidi, M. R. Feyzi, and M. Sabahi, "Design and analysis of a novel SEPIC-based multi-input DC / DC converter," vol. 10, no. 12, pp. 1393–1402, 2017.

[66] E. Babaei and E. M. S. Mahmoodieh, "Calculation of Output Voltage Ripple and Design Considerations of SEPIC Converter," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 3, pp. 1213–1222, 2014.

[67] A. Leki and D. M. Stipanović, "Hysteresis Switching Control of the Cuk Converter," *IEEE Transactions on Corcuits and systems -1*, vol. 63, no. 11, pp. 2048–2061, 2016.

[68] A. Leki and D. M. Stipanović, "Hysteresis Switching Control of the Cuk Converter Operating in Discontinuous Conduction Modes," *IEEE Transactions on Corcuits and systems-II: Express briefs*, vol. 64, no. 9, pp. 1077–1081, 2017.

[69] C. Wang, C. Lin, C. Lu, and J. Li, "Design and realisation of a zero-voltage transition pulse-width modulation interleaved boost power factor correction converter," *IET Power Electronics*, vol. 8, no. 8, pp. 1542–1551, 2015.

[70] C. Y. Yang, Y. C. Liu, P. J. Tseng, T. F. Pan, H. J. Chiu, and Y. K. Lo, "DSP-Based Interleaved Buck Power Factor Corrector with Adaptive Slope Compensation," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 8, pp. 4665–4677, 2015.

[71] O. Cipriano da Silva Filho, B. R. de Almeida, de Souza Oliveira Júnior. D, and T. R. Fernandes Neto, "High-Frequency Isolated AC DC AC Interleaved Converter for Power Quality Applications," *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 4594–4602, 2018.

[72] R. W. Erickson, J. Chen, and D. Maksimovic, "Analysis and Design of a Low-Stress Buck-Boost Converter in Universal-Input PFC Applications," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 320–329, 2006.

[73] C. Shi, A. Khaligh, and H. Wang, "Interleaved SEPIC Power Factor Preregulator Using Coupled Inductors In Discontinuous Conduction With Wide Output Voltage," *IEEE Transactions on Industry Applications*, vol. 52, no. 4, pp. 3461–3471, 2016.

[74] D. Patil, A. K. Rathore, and D. Srinivasan, "A Non-Isolated Bidirectional Soft Switching Current fed LCL Resonant dc / dc Converter to Interface Energy Storage in DC Microgrid," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 709–716, 2015.

[75] A. K. Rathore, D. R. Patil, and D. Srinivasan, "Non-isolated Bidirectional Soft-Switching Current-Fed LCL Resonant DC / DC Converter to Interface Energy Storage in DC Microgrid,"

IEEE Transactions on Industry Applications Applications, vol. 52, no. 2, pp. 1711–1722, 2016.

[76] S. Eren, M. Pahlevani, A. Bakhshai, and P. Jain, "An Adaptive Droop DC-Bus Voltage Controller for a Grid-Connected Voltage Source Inverter With LCL Filter," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 547–560, 2015.

[77] N. Mohan, T. M. Undeland, and W. P. Robbins, "Switching DC Power Supplies," in *Power Electronics- Converters, Applications and Design*, ch. 10, pp. 322–336, Singapore: John Wiley and sons Inc, Media Enhanced, 3 ed., 2003.

[78] L. Cao, "Type III compensator design for power converters," *https://www.powerelectronics.com/regulators/type-iii-compensator-design-power-converters*, vol. webpage, no. 2015-05-23, pp. 20–25, 2011.

[79] P. S. Nguyen, "Bilinear z-transformation and Pascal's triangle," *International Journal of Scientific and Engineering Research*, vol. 4, no. June, pp. 1974–1978, 2017.

[80] M. R. Rahimi, P. Parto, and P. Asadi, "Compensator Design Procedure for Buck Converter with Voltage -Mode Error-amplifier," *International Rectifier*, pp. 1–36, 2016.

[81] C. W. T. Mclyman, "Transformer and Inductor Design Handbook," in *Transformer and Inductor Design Handbook* (Martin O Thurston, ed.), ch. 3, 8, pp. 104–196, USA: Marcel Dekker, Inc., third ed., 2004.

[82] R. W. Erickson, "AC Equivalent Circuit Modeling," in *Fundamentals of Power Electronics*, ch. 7, pp. 213–221, Newyork, USA: Kluwer Academic Publishers, 2 ed., 2001.

[83] K.D.Joseph, A. E. Daniel, and A. Unnikrishnan, "Reduced Ripple Interleaved Cuk Converter with Phase Shifted PWM," in *Asian Control International Conference (ASCC 2015)*, (Malaysia), pp. 5–10, IEEE, 2015.

[84] Ferroxcube, "E55/28/21 E cores and accessories," *https://in.element14.com/ferroxcube/e55-28-21-3c90/ferrite-core-e-3c90/dp/2103338*, pp. 434–441, 2008.

[85] K. D. Joseph, A. E. Daniel, and A. Unnikrishnan, "Interleaved cuk converter with improved transient performance and reduced current ripple," *IET Journal of Engineering*, vol. 2017, no. 2, pp. 362–369, 2017.

[86] K. D. Joseph, A. E. Daniel, and A. Unnikrishnan, "Interleaved Cuk Converter with Reduced Switch Current," in *2018 International Conference on Power, Instrumentation, Control and Computing (PICC)*, (Thrissur), pp. 1–6, IEEE, 2018.

Appendix A

State Space Modelling of CCC

A.1 Introduction

The Cuk converter is modeled [82] using the state space technique in this section. The conventional Cuk converter shown in Fig. 3.1 is repeated as practical circuit in Fig. A.1 with the state variables marked. The state variables are
$i_{1a}(t)$, current through inductor L_{1a}
$i_{1b}(t)$, current through inductor L_{1b}
$v_{c1}(t)$, voltage across capacitor C_1 and
$v_{o1}(t)$ voltage across output capacitor C_{o1}. And the output variables are
$i_g(t)$, current through the the source and
$v_o(t)$, voltage across load resistance.

Let the equivalent resistances inductors L_{1a} and L_{1b} be given by r_{1a} and r_{1b} respectively. Similarly the capacitors C_1 and C_{o1} have

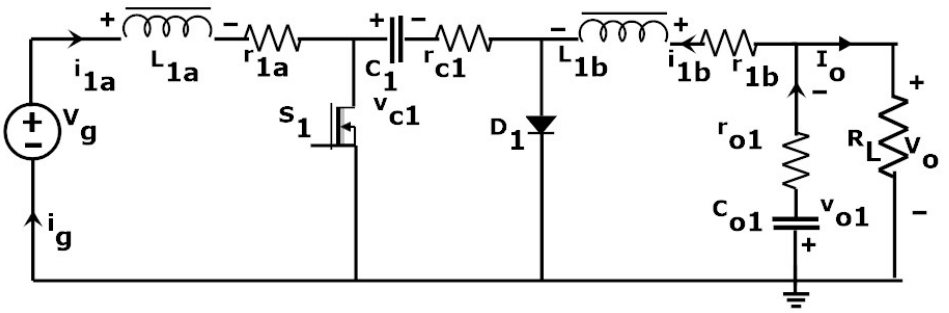


Fig. A.1: The circuit diagram of Conventional Cuk converter

equivalent series resistances respectively as r_{c1} and r_{o1}. The variables V_g, i_g, R_L, V_o, I_o respectively represent input voltage, input current, load resistance, output voltage and output current. The capacitor C_1 acts as primary means of storing and transferring energy from the input to the output. The average voltage across inductor V_{L1a} and V_{L1b} are zero at steady state. The capacitor C_1 is designed in such a way that it transfers the constant voltage. The state space model is derived considering two modes of operation viz. Mode 1 - Switch S_1 ON and Mode 2 - Switch S_1 OFF

A.2 Mode 1 - Switch S_1 ON

When the switch S_1 is in ON position as shown in the circuit diagram of Fig.A.2, the voltage across inductor L_{1a} is given by the equation (A.1)

$$L_{1a}\frac{di_{1a}(t)}{dt} + r_{1a}i_{1a}(t) = v_g(t) \tag{A.1}$$

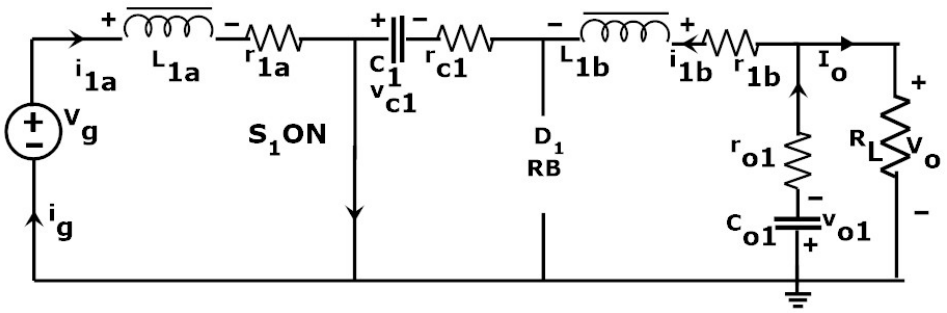


Fig. A.2: The circuit diagram of practical CCC when the switch S1 is in ON state(D_1 RB - Diode in Reverse Bias)

The current through C_{o1} is given by the equation (A.2)

$$(i_{1b}(t) - C_{o1}\frac{dv_{o1}(t)}{dt})R_L = r_{o1}C_{o1}\frac{dv_{o1}(t)}{dt} + v_{o1}(t) \tag{A.2}$$

The voltage across L_{1b} is given by the equation (A.3)

$$-v_{o1}(t) - r_{o1}C_{o1}\frac{dv_{o1}(t)}{dt} - L_{1b}\frac{di_{1b}(t)}{dt} - r_{1b}i_{1b}(t) + v_{c1}(t) - r_{c1}i_{1b}(t) = 0 \tag{A.3}$$

The current through C_1 is given by A.4

$$C_1\frac{dv_{c1}(t)}{dt} = -i_{1b}(t) \tag{A.4}$$

The current through the source is given by A.5

$$i_g(t) = i_{1a}(t) \tag{A.5}$$

The voltage across load resistance is given by A.6

$$v_o(t) = -(v_{o1}(t) + r_{o1}C_{o1}\frac{dv_{o1}(t)}{dt}) \tag{A.6}$$

Rearranging the equations from A.1 to A.4 and the state equations are

$$\frac{di_{1a}(t)}{dt} = -\frac{r_{1a}}{L_{1a}} i_{1a}(t) + \frac{v_g(t)}{L_{1a}} \tag{A.7}$$

$$\frac{di_{1b}(t)}{dt} = [-r_{1b} - r_{c1} - \frac{r_{o1}R_L}{R_L + r_{o1}}](\frac{i_{1b}(t)}{L_{1b}}) + \frac{v_{c1}(t)}{L_{1b}} + \frac{1}{L_{1b}}[-1 + \frac{r_{o1}}{(R_L + r_{o1})}]v_{o1}(t) \tag{A.8}$$

$$\frac{dv_{c1}(t)}{dt} = -\frac{i_{1b}(t)}{C_1} \tag{A.9}$$

$$\frac{dv_{o1}(t)}{dt} = \frac{i_{1b}(t)R_L}{(R_L + r_{o1})C_{o1}} - \frac{v_{o1}(t)}{(R_L + r_{o1})C_{o1}} \tag{A.10}$$

Writing the state equation in standard form

$$\frac{dx(t)}{dt} = A_1 x(t) + B_1 u(t) \tag{A.11}$$

in matrix form

$$\begin{bmatrix} \frac{di_{1a}(t)}{dt} \\ \frac{di_{1b}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{o1}(t)}{dt} \end{bmatrix} = \begin{bmatrix} A1_{11} & 0 & 0 & 0 \\ 0 & A1_{22} & A1_{23} & A1_{24} \\ 0 & A1_{32} & 0 & 0 \\ 0 & A1_{42} & 0 & A1_{44} \end{bmatrix} \begin{bmatrix} i_{1a}(t) \\ i_{1b}(t) \\ v_{c1}(t) \\ v_{o1}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{1a}} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_g(t)$$

where
$A1_{11} = -\frac{r_{1a}}{L_{1a}}$, $A1_{22} = -[r_{1b} + r_{c1} + \frac{r_{o1}R_L}{R_L + r_{o1}}](\frac{1}{L_{1b}})$, $A1_{23} = -\frac{1}{L_{1b}}$,
$A1_{24} = \frac{1}{L_{1b}}[-1 + \frac{r_{o1}}{(R_L + r_{o1})}]$, $A1_{32} = -\frac{1}{C_1}$
$A1_{42} = \frac{R_L}{(R_L + r_{o1})C_{o1}}$, $A1_{44} = -\frac{1}{(R_L + r_{o1})C_{o1}}$,
The output equations from A.5 and A.6are given by

$$i_g(t) = i_{1a}(t) \tag{A.12}$$

$$v_o(t) = -\frac{r_{o1}R_L i_{1b}(t)}{R_L + r_{o1}} - \frac{R_L v_{o1}(t)}{R_L + r_{o1}} \tag{A.13}$$

The output equation takes the standard form given by

$$\frac{dy(t)}{dt} = C_{mod1}x(t) + E_1 u(t) \tag{A.14}$$

in matrix form is

$$\begin{bmatrix} i_g(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & -\frac{r_{o1}R_L}{R_L + r_{o1}} & 0 & -\frac{R_L}{R_L + r_{o1}} \end{bmatrix} \begin{bmatrix} i_{1a}(t) \\ i_{1b}(t) \\ v_{c1}(t) \\ v_{o1}(t) \end{bmatrix} + \begin{bmatrix} 0 \end{bmatrix} v_g(t)$$

Now the rows in output matrix are

$$\begin{bmatrix} C_{mod1R_1} \\ C_{mod1R_2} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & -\frac{r_{o1}R_L}{R_L + r_{o1}} & 0 & -\frac{R_L}{R_L + r_{o1}} \end{bmatrix}$$

The first and second rows of output matrix respectively represent input current $i_g(t)$ and output voltage $v_o(t)$. The output is regulated by direct duty ratio control by taking the transfer function of $v_o(s)/d(s)$.

A.3 Mode 2 - Switch S_1 OFF

The circuit diagram when the switch S_1 is OFF is shown in Fig.A.3.

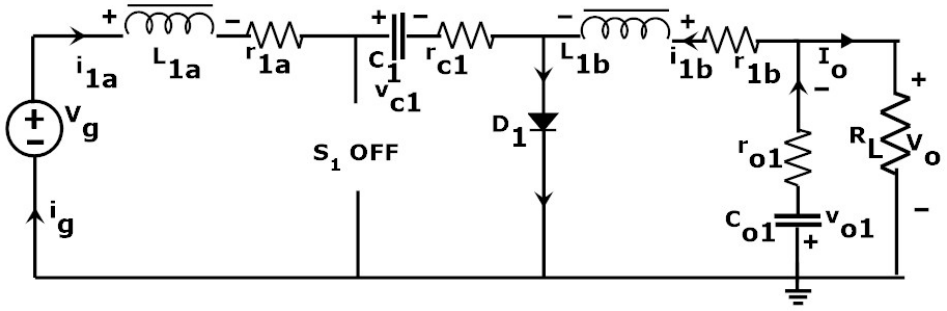


Fig. A.3: The circuit diagram of CCC when the switch S_1 is OFF

The voltage across inductor L_{1a} is given by the equation (A.15)

$$L_{1a}\frac{di_{1a}(t)}{dt} = -(r_{1a} + r_{c1})i_{1a}(t) - v_{c1}(t) + v_g(t) \tag{A.15}$$

The current through C_{o1} is given by the equation (A.16)

$$r_{o1}C_{o1}\frac{dv_{o1}(t)}{dt} + v_{o1}(t) - (i_{1b}(t) - C_{o1}\frac{dv_{o1}(t)}{dt})R_L = 0 \tag{A.16}$$

The voltage across L_{1b} is given by the equation (A.17)

$$-v_{o1}(t) - r_{o1}C_{o1}\frac{dv_{o1}(t)}{dt} - L_{1b}\frac{di_{1b}(t)}{dt} - r_{1b}i_{1b}(t) = 0 \tag{A.17}$$

The current through C_1 is given by the equation A.18

$$C_1\frac{dv_{c1}(t)}{dt} = i_{1a}(t) \tag{A.18}$$

The current through the source is given by the equation (A.19)

$$i_g(t) = i_{1a}(t) \tag{A.19}$$

The voltage across load resistance is given by the equation (A.20)

$$v_o(t) = -(v_{o1}(t) + r_{o1}C_{o1}\frac{dv_{o1}(t)}{dt}) \tag{A.20}$$

Rearranging the equations from (A.15) to (A.18) and the state equations are

$$\frac{di_{1a}(t)}{dt} = -\frac{r_{1a} + r_{c1}i_{1a}(t)}{L_{1a}} - \frac{v_{c1}(t)}{L_{1a}} + \frac{v_g(t)}{L_{1a}} \tag{A.21}$$

$$\frac{di_{1b}(t)}{dt} = [-r_{1b} - \frac{r_{o1}R_L}{R_L + r_{o1}}](\frac{i_{1b}(t)}{L_{1b}}) - \frac{R_L v_{o1}(t)}{(R_L + r_{o1})L_{1b}} \tag{A.22}$$

$$\frac{dv_{c1}(t)}{dt} = -\frac{i_{1a}(t)}{C_1} \tag{A.23}$$

$$\frac{dv_{o1}(t)}{dt} = \frac{i_{1b}(t)R_L}{(R_L + r_{o1})C_{o1}} - \frac{v_{o1}(t)}{(R_L + r_{o1})C_{o1}} \tag{A.24}$$

Writing the state equations

$$\frac{dx(t)}{dt} = A_2x(t) + B_2u(t) \tag{A.25}$$

in matrix form

$$\begin{bmatrix} \frac{di_{1a}(t)}{dt} \\ \frac{di_{1b}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{o1}(t)}{dt} \end{bmatrix} = \begin{bmatrix} A2_{11} & 0 & A2_{13} & 0 \\ 0 & A2_{22} & 0 & A2_{24} \\ A2_{31} & 0 & 0 & 0 \\ 0 & A2_{42} & 0 & A2_{44} \end{bmatrix} \begin{bmatrix} i_{1a}(t) \\ i_{1b}(t) \\ v_{c1}(t) \\ v_{o1}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{1a}} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_g(t)$$

Where
$A2_{11} = -\frac{r_{1a} + r_{o1}}{L_{1a}}$, $A2_{13} = -\frac{1}{L_{1a}}$, $A2_{22} = -[r_{1b} + \frac{r_{o1}R_L}{R_L + r_{o1}}](\frac{1}{L_{1b}})$
$A2_{24} = \frac{1}{L_{1b}}[-\frac{R_L}{R_L + r_{o1})}]$, $A2_{31} = \frac{1}{C_1}$,
$A2_{42} = \frac{R_L}{(R_L + r_{o1})C_{o1}}$, $A2_{44} = -\frac{1}{(R_L + r_{o1})C_{o1}}$

The output equations from (A.19) and (A.20) are given by

$$i_g(t) = i_{1a}(t) \tag{A.26}$$

$$v_o(t) = -\frac{r_{o1}R_L i_{1b}(t)}{R_L + r_{o1}} - \frac{R_L v_{o1}(t)}{R_L + r_{o1}} \tag{A.27}$$

The output equation takes standard form given by

$$\frac{dy(t)}{dt} = C_{mod2}x(t) + E_2u(t) \tag{A.28}$$

in matrix form is

$$\begin{bmatrix} i_g(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & -\frac{r_{o1}R_L}{R_L + r_{o1}} & 0 & -\frac{R_L}{R_L + r_{o1}} \end{bmatrix} \begin{bmatrix} i_{1a}(t) \\ i_{1b}(t) \\ v_{c1}(t) \\ v_{o1}(t) \end{bmatrix} + \begin{bmatrix} 0 \end{bmatrix} v_g(t)$$

Now the rows in output matrix are

$$\begin{bmatrix} C_{mod2R_1} \\ C_{mod2R_2} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & -\frac{r_{o1}R_L}{R_L + r_{o1}} & 0 & -\frac{R_L}{R_L + r_{o1}} \end{bmatrix}$$

The first and second rows of output matrix respectively represent input current $i_g(t)$ and output voltage $v_o(t)$.

Appendix B

State Space Modelling of Proposed ICC

B.1 Mode -1 S_1 ON and S_2 OFF $(t_0 - t_1)$

With reference to the Fig.5.3 the state space modelling of Modified ICC in Mode-1 is given as follows.

The state equation for inductor L_{1a} is given by (B.1)

$$\frac{di_{1a}(t)}{dt} = -\frac{r_{1a}i_{1a}(t)}{L_{1a}} + \frac{V_g}{L_{1a}} \tag{B.1}$$

The state equation for C_1 is given by (B.2)

$$\frac{dv_{c1}(t)}{dt} = -\frac{i_{1b}(t)}{C_1} \tag{B.2}$$

The state equation for C_2 is given by (B.3)

$$\frac{dv_{c2}(t)}{dt} = \frac{i_{2a}(t)}{C_2} \tag{B.3}$$

The voltage across L_{2a} is given by Eqn B.4,

$$\frac{di_{2a}(t)}{dt} = -(\frac{r_{2a} + r_{c2}}{L_{2a}})i_{2a}(t) - \frac{v_{c2}(t)}{L_{2a}} + \frac{v_g(t)}{L_{2a}} \tag{B.4}$$

The state equation for capacitor C_{o2} is given by Eqn. B.5.

$$\begin{aligned} \frac{dv_{o2}(t)}{dt} &= \frac{r_{o1}}{(R_L r_{o1} + r_{o2} r_{o1} + r_{o2} R_L) C_{o2}} * \\ [R_L i_{1b}(t) + R_L i_{2b}(t) + \frac{v_{o1}(t) R_L}{r_{o1}} - \frac{v_{o2}(t)(1 + R_L)}{r_{o1}}] \end{aligned} \tag{B.5}$$

Writing equation for Capacitor C_{o1} as Eqn.B.6

$$\begin{aligned} \frac{dv_{o1}(t)}{dt} &= \frac{r_{o2}}{(R_L r_{o2} + r_{o2} r_{o1} + r_{o1} R_L) C_{o1}} * \\ [R_L i_{1b}(t) + R_L i_{2b}(t) + \frac{v_{o2}(t) R_L}{r_{o2}} - \frac{v_{o1}(t)(1 + R_L)}{r_{o2}}] \end{aligned} \tag{B.6}$$

The voltage equation for L_{1b} is given by (B.7).

$$\begin{aligned} \frac{di_{1b}(t)}{dt} = [-\frac{i_{1b}(t)}{L_{1b}}][r_{1b} - r_{c1} + \frac{r_{o1} r_{o2} R_L}{(R_L r_{o2} + R_L r_{o1} + r_{o1} r_{o2})}] \\ -[\frac{i_{2b}(t)}{L_{1b}}]\frac{r_{o1} R_L}{(R_L r_{o2} + r_{o1} R_L + r_{o1} r_{o2})} \\ -[\frac{v_{o1}(t)}{L_{1b}}]\frac{R_L r_{o2}}{(R_L r_{o2} + r_{o1} R_L + r_{o1} r_{o2})} \\ -[\frac{v_{o2}(t)}{L_{1b}}]\frac{R_L r_{o1}}{(R_L r_{o2} + r_{o1} R_L + r_{o1} r_{o2})} + [\frac{v_{c1}(t)}{L_{1b}}] \end{aligned} \tag{B.7}$$

Voltage equation for L_{2b} is given by Eqn. B.8

$$\begin{aligned}\frac{di_{2b}(t)}{dt} = [-\frac{i_{1b}(t)}{L_{2b}}][-\frac{r_{o1}r_{o2}R_L}{(R_Lr_{o2}+R_Lr_{o1}+r_{o1}r_{o2})}] \\ [\frac{i_{2b}(t)}{L_{2b}}][-\frac{r_{o1}r_{o2}R_L}{(R_Lr_{o2}+R_Lr_{o1}+r_{o1}r_{o2})} - r_{2b}] \\ [\frac{v_{o1}(t)}{L_{2b}}][-\frac{r_{o2}R_L}{(R_Lr_{o2}+R_Lr_{o1}+r_{o1}r_{o2})}] \\ [\frac{v_{o2}(t)}{L_{2b}}][-\frac{r_{o1}R_L}{(R_Lr_{o2}+R_Lr_{o1}+r_{o1}r_{o2})}]\end{aligned} \tag{B.8}$$

These are the eight state equations to form the matrices for Mode -1. Writing the state equations (B.1), (B.7), (B.4), (B.8), (B.2), (B.3), (B.6) and (B.5) in matrix form

The state space model of ICC in Mode 1 is given below.

$$\begin{bmatrix} \frac{di_{1a}(t)}{dt} \\ \frac{di_{1b}(t)}{dt} \\ \frac{di_{2a}(t)}{dt} \\ \frac{di_{2b}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \\ \frac{dv_{o1}(t)}{dt} \\ \frac{dv_{o2}(t)}{dt} \end{bmatrix} = \begin{bmatrix} A1_{11} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & A1_{22} & 0 & A1_{24} & A1_{25} & 0 & A1_{27} & A1_{28} \\ 0 & 0 & A1_{33} & 0 & 0 & A1_{36} & 0 & 0 \\ 0 & A1_{42} & 0 & A1_{44} & 0 & 0 & A1_{47} & A1_{48} \\ 0 & A1_{52} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & A1_{63} & 0 & 0 & 0 & 0 & 0 \\ 0 & A1_{72} & 0 & A1_{74} & 0 & 0 & A1_{77} & A1_{78} \\ 0 & A1_{82} & 0 & A1_{84} & 0 & 0 & A1_{87} & A1_{88} \end{bmatrix} \begin{bmatrix} i_{1a}(t) \\ i_{1b}(t) \\ i_{2a}(t) \\ i_{2b}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{o1}(t) \\ v_{o2}(t) \end{bmatrix}$$
$$+ \begin{bmatrix} \frac{1}{L_{1a}} \\ 0 \\ \frac{1}{L_{2a}} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} v_g(t) \end{bmatrix}$$

where

$$A1_{11} = \frac{-r_{1a}}{L_{1a}},$$

$$A1_{22} = \frac{(-R_L * r_{o1} * r_{o2})}{L_{1b} * (R_L * r_{o2} + r_{o1} * r_{o2} + R_L * r_{o1})} - \frac{r_{1b}}{L_{1b}} + \frac{r_{c1}}{L_{1b}}$$

$$A1_{24} = \frac{(-R_L * r_{o1} * r_{o2})}{L_{1b} * (R_L * r_{o2} + r_{o1} * r_{o2} + R_L * r_{o1})},\ A1_{25} = \frac{1}{L_{1b}}$$

$$A1_{27} = \frac{R_L * r_{o2}}{(R_L * r_{o2} + r_{o1} * r_{o2} + R_L * r_{o1}) * L_{1b}} - \frac{1}{L_{1b}}$$
$$A1_{28} = \frac{-R_L * r_{o1}}{L_{1b} * (R_L * r_{o2} + r_{o1} * r_{o2} + R_L * r_{o1})}, A1_{33} = \frac{-r_{2a} - r_{c2}}{L_{2a}};$$
$$A1_{36} = \frac{-1}{L_{2a}}, A1_{42} = \frac{(-R_L * r_{o1} * r_{o2})}{L_{2b} * (R_L * r_{o2} + r_{o1} * r_{o2} + R_L * r_{o1})}$$
$$A1_{44} = \frac{-R_L * r_{o1} * r_{o2}}{L_{2b} * (R_L * r_{o2} + r_{o1} * r_{o2} + R_L * r_{o1})} - \frac{r_{2b}}{L_{2b}}$$
$$A1_{47} = \frac{-R_L * r_{o2}}{L_{2b} * (R_L * r_{o2} + r_{o1} * r_{o2} + R_L * r_{o1})}$$
$$A1_{48} = \frac{r_{o1} * R_L}{L_{2b} * (R_L * r_{o2} + r_{o1} * r_{o2} + R_L * r_{o1})} - \frac{1}{L_{2b}}, A1_{52} = \frac{-1}{C_1},$$
$$A1_{63} = \frac{1}{C_2}, A1_{72} = A1_{74} = \frac{R_L * r_{o2}}{C_{o1} * (R_L * r_{o2} + r_{o1} * r_{o2} + R_L * r_{o1})}$$
$$A1_{77} = \frac{-(R_L + r_{o2})}{C_{o1} * (R_L * r_{o2} + r_{o1} * r_{o2} + R_L * r_{o1})}$$
$$A1_{78} = \frac{R_L}{C_{o1} * (R_L * r_{o2} + r_{o1} * r_{o2} + R_L * r_{o1})}$$
$$A1_{82} = A1_{84} = \frac{R_L * r_{o1}}{C_{o2} * (R_L * r_{o2} + r_{o1} * r_{o2} + R_L * r_{o1})}$$
$$A1_{87} = \frac{R_L}{C_{o2} * (R_L * r_{o2} - r_{o1} * r_{o2} + R_L * r_{o1})}$$
$$A1_{88} = \frac{-(R_L + r_{o1})}{C_{o2} * (R_L * r_{o2} + r_{o1} * r_{o2} + R_L * r_{o1})}$$

And the output equation (row wise) in matrix is

$$\begin{bmatrix} i_g(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & C1_{22} & 0 & C1_{24} & 0 & 0 & C1_{27} & C1_{28} \end{bmatrix} \begin{bmatrix} i_{1a}(t) \\ i_{1b}(t) \\ i_{2a}(t) \\ i_{2b}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{o1}(t) \\ v_{o2}(t) \end{bmatrix}$$

Where rows $i_g(t)$ and $v_o(t)$ are assigned as $C_{mode1R1}$ and $C_{mode1R2}$ respectively. $C1_{22} = C1_{24} = -\dfrac{R_L * r_{o1} * r_{o2}}{(R_L * r_{o2} + r_{o1} * r_{o2} + R_L * r_{o1})}$,
$C1_{27} = -\dfrac{R_L * r_{o2}}{(R_L * r_{o2} + r_{o1} * r_{o2} + R_L * r_{o1})}$,
$C1_{28} = -\dfrac{R_L * r_{o1}}{(R_L * r_{o2} + r_{o1} * r_{o2} + R_L * r_{o1})}$

B.2 Mode-2 S_1 and S_2 OFF $(t_1 - t_2)$

Similar to Mode -1, the state equations can be written for Mode -2. The state space model in Mode-2 when both switches S_1 and S_2 in

OFF states is given by

$$\begin{bmatrix} \frac{di_{1a}(t)}{dt} \\ \frac{di_{1b}(t)}{dt} \\ \frac{di_{2a}(t)}{dt} \\ \frac{di_{2b}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \\ \frac{dv_{o1}(t)}{dt} \\ \frac{dv_{o2}(t)}{dt} \end{bmatrix} = \begin{bmatrix} A2_{11} & 0 & 0 & 0 & A2_{15} & 0 & 0 & 0 \\ 0 & A2_{22} & 0 & A2_{24} & 0 & 0 & A2_{27} & A2_{28} \\ 0 & 0 & A2_{33} & 0 & 0 & A2_{36} & 0 & 0 \\ 0 & A2_{42} & 0 & A2_{44} & 0 & 0 & A2_{47} & A2_{48} \\ A2_{51} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & A2_{63} & 0 & 0 & 0 & 0 & 0 \\ 0 & A2_{72} & 0 & A2_{74} & 0 & 0 & A2_{77} & A2_{78} \\ 0 & A2_{82} & 0 & A2_{84} & 0 & 0 & A2_{87} & A2_{88} \end{bmatrix} \begin{bmatrix} i_{1a}(t) \\ i_{1b}(t) \\ i_{2a}(t) \\ i_{2b}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{o1}(t) \\ v_{o2}(t) \end{bmatrix}$$

$$+ \begin{bmatrix} \frac{1}{L_{1a}} \\ 0 \\ \frac{1}{L_{2a}} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} v_g(t) \end{bmatrix}$$

where $A2_{11} = \dfrac{-r_{1a} - r_{c1}}{L_{1a}}$, $A2_{15} = \dfrac{-1}{L_{1a}}$,

$A2_{22} = -\dfrac{r_{1b}}{L_{1b}} - \dfrac{R_L * r_{o1} * r_{o2}}{L_{1b} * (R_L * r_{o2} + r_{o1} * r_{o2} + R_L * r_{o1})}$

$A2_{24} = A1_{24}$, $A2_{27} = A1_{27}$, $A2_{28} = A1_{28}$, $A2_{33} = A1_{33}$, $A2_{36} = A1_{36}$,

$A2_{42} = A1_{42}$, $A2_{44} = A1_{44}$, $A2_{47} = A1_{47}$, $A2_{48} = A1_{48}$, $A2_{51} = \dfrac{1}{C_1}$,

$A2_{63} = A1_{63}$, $A2_{72} = A2_{74} = A1_{72}$, $A2_{77} = A1_{77}$, $A2_{78} = A1_{78}$,
$A2_{82} = A2_{84} = A1_{82}$, $A2_{87} = A1_{87}$, $A2_{88} = A1_{88}$.

And the equation for output is

$$\begin{bmatrix} i_g(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & C2_{22} & 0 & C2_{24} & 0 & 0 & C2_{27} & C2_{28} \end{bmatrix} \begin{bmatrix} i_{1a}(t) \\ i_{1b}(t) \\ i_{2a}(t) \\ i_{2b}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{o1}(t) \\ v_{o2}(t) \end{bmatrix}$$

where rows $i_g(t)$ and $v_o(t)$ are assigned as $C_{mode2R1}$ and $C_{mode2R2}$ respectively,
$C2_{22} = C2_{24} = C1_{22}, C2_{27} = C1_{27}, C2_{28} = C1_{28}$

B.3 Mode-3 S_1 OFF and S_2 ON $(t_2 - t_3)$

Writing the state equation in matrix form when the switiches S_1 in OFF and S_2 in ON positions

$$\begin{bmatrix} \frac{di_{1a}(t)}{dt} \\ \frac{di_{1b}(t)}{dt} \\ \frac{di_{2a}(t)}{dt} \\ \frac{di_{2b}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \\ \frac{dv_{o1}(t)}{dt} \\ \frac{dv_{o2}(t)}{dt} \end{bmatrix} = \begin{bmatrix} A3_{11} & 0 & 0 & 0 & A3_{15} & 0 & 0 & 0 \\ 0 & A3_{22} & 0 & A3_{24} & 0 & 0 & A3_{27} & A3_{28} \\ 0 & 0 & A3_{33} & 0 & 0 & 0 & 0 & 0 \\ 0 & A3_{42} & 0 & A3_{44} & 0 & A3_{46} & A3_{47} & A3_{48} \\ A3_{51} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & A3_{64} & 0 & 0 & 0 & 0 \\ 0 & A3_{72} & 0 & A3_{74} & 0 & 0 & A3_{77} & A3_{78} \\ 0 & A3_{82} & 0 & A3_{84} & 0 & 0 & A3_{87} & A3_{88} \end{bmatrix} \begin{bmatrix} i_{1a}(t) \\ i_{1b}(t) \\ i_{2a}(t) \\ i_{2b}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{o1}(t) \\ v_{o2}(t) \end{bmatrix}$$

$$+ \begin{bmatrix} \frac{1}{L_{1a}} \\ 0 \\ \frac{1}{L_{2a}} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} v_g(t) \end{bmatrix}$$

Where
$A3_{11} = A2_{11}$, $A3_{15} = A2_{15}$, $A3_{22} = A2_{22}$, $A3_{24} = A2_{24}$,
$A3_{27} = A2_{27}$, $A3_{28} = A2_{28}$, $A3_{33} = \frac{-r_{2a}}{L_{2a}}$;

$A3_{42} = A2_{42}$, $A3_{44} = \dfrac{-r_{2b} + r_{c2}}{L_{2b}} - \dfrac{r_{o1}r_{o2}R_L}{(R_L r_{o1} + r_{o1}r_{o2} + r_{o2}R_L)L_{2b}}$,
$A3_{46} = \dfrac{1}{L_{2b}}$, $A3_{47} = A2_{47}$, $A3_{48} = A2_{48}$, $A3_{51} = A2_{51}$, $A3_{64} = \dfrac{-1}{C_2}$,
$A3_{72} = A3_{74} = A2_{72}$, $A3_{77} = A2_{77}$, $A3_{78} = A2_{78}$, $A3_{82} = A3_{84} = A2_{82}$
$A3_{87} = A2_{87}$ $A3_{88} = A2_{88}$.
The output is given by equations B.9 and B.10

$$i_g(t) = i_{1a}(t) + i_{2a}(t) \tag{B.9}$$

$$\begin{aligned} v_o(t) = -[&\frac{r_{o1}r_{o2}R_L}{(R_L r_{o2} + r_{o1}r_{o2} + r_{o1}R_L)} i_{1b}(t) \\ &- \frac{R_L r_{o1}r_{o2}}{(R_L r_{o2} + r_{o1}r_{o2} + r_{o1}R_L)} i_{2b}(t) \\ &[-1 + \frac{(R_L - r_{o2})r_{o1}}{(R_L r_{o2} + r_{o1}r_{o2} + r_{o1}R_L)}] v_{o1}(t) \\ &- \frac{R_L r_{o1}}{(R_L r_{o2} + r_{o1}r_{o2} + r_{o1}R_L)} v_{o2}(t)] \end{aligned} \tag{B.10}$$

The output in matrix form is

$$\begin{bmatrix} i_g(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & C3_{22} & 0 & C3_{24} & 0 & 0 & C3_{27} & C3_{28} \end{bmatrix} \begin{bmatrix} i_{1a}(t) \\ i_{1b}(t) \\ i_{2a}(t) \\ i_{2b}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{o1}(t) \\ v_{o2}(t) \end{bmatrix} + \begin{bmatrix} 0 \end{bmatrix} \begin{bmatrix} v_g(t) \end{bmatrix}$$

Where $C3_{22} = C3_{24} = C1_{22}$ $C3_{27} = C1_{27}$ $C3_{28} = C1_{28}$ Also rows $i_g(t)$ and $v_o(t)$ are assigned as $C_{mode3R1}$ and $C_{mode3R2}$ respectively.

B.4 Mode 4 - S_1 and S_2 OFF $(t_3 - t_4)$

This mode is repetition of mode 2 (shown in section B.2) and the matrices termed as A_4, B_4 and C_4. Also rows $i_g(t)$ and $v_o(t)$ are assigned as $C_{mode4R1}$ and $C_{mode4R2}$ respectively.

Appendix C

State Space Modelling of Modified ICC

C.1 Mode 1 - S_1 ON and S_2 OFF $(t_0 - t_1)$

With reference to the Fig.7.7 the state space modelling of Modified ICC in Mode-1 is given as follows.

The state equation for inductor L_{1a} is given by (C.1)

$$\frac{di_{1a}(t)}{dt} = -\frac{r_{1a}i_{1a}(t)}{L_{1a}} + \frac{V_g}{L_{1a}} \tag{C.1}$$

The state equation for C_1 is given by (C.2)

$$\frac{dv_{c1}(t)}{dt} = -\frac{i_{1b}(t)}{C_1} - \frac{i_{2a}(t)}{C_1} - \frac{i_{2b}(t)}{C_1} \tag{C.2}$$

The state equation for C_2 is given by (C.3)

$$\frac{dv_{c2}(t)}{dt} = \frac{i_{2a}(t)}{C_2} \tag{C.3}$$

The voltage across L_{2a} is given by

$$\begin{aligned} v_g(t) - L_{2a}\frac{di_{2a}(t)}{dt} - r_{2a}i_{2a}(t) - v_{c2}(t) \\ -r_{c2}C2\frac{dv_{c2}(t)}{dt} + r_{c1}C1\frac{dv_{c1}(t)}{dt} + v_{c1}(t) = 0 \end{aligned} \tag{C.4}$$

Substituting equations (C.2) and (C.3) in the above expression and state equation for L_{2a} is given by (C.5).

$$\begin{aligned} \frac{di_{2a}(t)}{dt} = -\frac{r_{c1}}{L_{2a}}i_{1b}(t) - (\frac{r_{2a}+r_{c1}+r_{c2}}{L_{2a}})i_{2a}(t) \\ -\frac{r_{c1}}{L_{2a}}i_{2b}(t) + \frac{v_{c1}(t)}{L_{2a}} - \frac{v_{c2}(t)}{L_{2a}} + \frac{v_g(t)}{L_{2a}} \end{aligned} \tag{C.5}$$

The expressions for voltage across load is given by

$$v_o(t) = r_{o1}C_{o1}\frac{dv_{o1}(t)}{dt} + v_{o1}(t) + r_{o2}C_{o2}\frac{dv_{o2}(t)}{dt} + v_{o2}(t)$$

and

$$v_o(t) = (i_{2b}(t) - C_{o2}\frac{dv_{o2}(t)}{dt})R_L$$

Equating above two expressions and the state equation for capacitor C_{o2} is given by (C.6).

$$\frac{dv_{o2}(t)}{dt} = \frac{1}{(R_L + r_{o2} + r_{o1})C_{o2}}[-r_{o1}i_{1b} + R_L i_{2b} - v_{o1} - v_{o2}] \tag{C.6}$$

Writing equation for Capacitor C_{o1}

$$\frac{dv_{o1}(t)}{dt} = \frac{1}{(R_L + r_{o2} + r_{o1})C_{o1}}[(R_L + r_{o2})i_{1b} + R_L i_{2b} - v_{o1} - v_{o2}] \quad \text{(C.7)}$$

The voltage equation for L_{1b} is

$$\begin{aligned} &-r_{o1}C_{o1}\frac{dv_{o1}(t)}{dt} - v_{o1}(t) - r_{1b}i_{1b}(t) - L_{1b}\frac{di_{1b}(t)}{dt} \\ &+r_{c1}C_1\frac{dv_{c1}(t)}{dt} + v_{c1}(t) = 0 \end{aligned}$$

Substituting equation (C.2) and (C.7) in the above expression and state equation for L_{1b} is given by (C.8).

$$\begin{aligned} \frac{di_{1b}(t)}{dt} &= (-r_{1b} - r_{c1} - \frac{r_{o1}(R_L + r_{o2})}{(R_L + r_{o2} + r_{o1})})[\frac{i_{1b}(t)}{L_{1b}}] - \frac{r_{c1}}{L_{1b}}i_{2a}(t) \\ &-(r_{c1} + \frac{r_{o1}R_L}{(R_L + r_{o2} + r_{o1})})[\frac{i_{2b}(t)}{L_{1b}}] + \frac{v_{c1}(t)}{L_{1b}} \\ &-\frac{(R_L + r_{o2})}{(R_L + r_{o2} + r_{o1})}[\frac{v_{o1}(t)}{L_{1b}}] + \frac{r_{o1}}{(R_L + r_{o2} + r_{o1})}[\frac{v_{o2}(t)}{L_{1b}}] \end{aligned} \quad \text{(C.8)}$$

Voltage equation for L_{2b} is given by

$$\begin{aligned} &vo1(t) - r_{o1}C_{o1}\frac{dv_{o1}(t)}{dt} - r_{o2}C_{o2}\frac{dv_{o2}(t)}{dt} - v_{o2}(t) - r_{2b}i_{2b}(t) \\ &-L_{2b}\frac{di_{2b}(t)}{dt} + r_{c1}C_1\frac{dv_{c1}(t)}{dt} + v_{c1}(t) = 0 \end{aligned}$$

Substituting equations (C.6), (C.7) and (C.2) in the above expression

to obtain state equation (C.9) for the inductor L_{2b}.

$$\frac{di_{2b}(t)}{dt} = (-r_{c1} - \frac{r_{o1}R_L}{(R_L + r_{o2} + r_{o1})})[\frac{i_{1b}(t)}{L_{2b}}] - \frac{r_{c1}}{L_{2b}} i_{2a}(t)$$
$$-(r_{2b} - r_{c1} - \frac{(r_{o1} + r_{o2})R_L}{(R_L + r_{o2} + r_{o1})})[\frac{i_{2b}(t)}{L_{2b}}] + \frac{v_{c1}(t)}{L_{2b}}$$
$$-\frac{(R_L)}{(R_L + r_{o2} + r_{o1})}[\frac{v_{o1}(t)}{L_{2b}}] - \frac{R_L}{(R_L + r_{o2} + r_{o1})}[\frac{v_{o2}(t)}{L_{2b}}] \tag{C.9}$$

Writing the state equations (C.1), (C.8), (C.5), (C.9), (C.2), (C.3),

(C.7) and (C.6) in matrix form

$$\begin{bmatrix} \frac{di_{1a}(t)}{dt} \\ \frac{di_{1b}(t)}{dt} \\ \frac{di_{2a}(t)}{dt} \\ \frac{di_{2b}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \\ \frac{dv_{o1}(t)}{dt} \\ \frac{dv_{o2}(t)}{dt} \end{bmatrix} = \begin{bmatrix} A1_{11} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & A1_{22} & A1_{23} & A1_{24} & A1_{25} & 0 & A1_{27} & A1_{28} \\ 0 & A1_{32} & A1_{33} & A1_{34} & A1_{35} & A1_{36} & 0 & 0 \\ 0 & A1_{42} & A1_{43} & A1_{44} & A1_{45} & 0 & A1_{47} & A1_{48} \\ 0 & A1_{52} & A1_{53} & A1_{54} & 0 & 0 & 0 & 0 \\ 0 & 0 & A1_{63} & 0 & 0 & 0 & 0 & 0 \\ 0 & A1_{72} & 0 & A1_{74} & 0 & 0 & A1_{77} & A1_{78} \\ 0 & A1_{82} & 0 & A1_{84} & 0 & 0 & A1_{87} & A1_{88} \end{bmatrix} \begin{bmatrix} i_{1a}(t) \\ i_{1b}(t) \\ i_{2a}(t) \\ i_{2b}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{o1}(t) \\ v_{o2}(t) \end{bmatrix}$$

$$+ \begin{bmatrix} \frac{1}{L_{1a}} \\ 0 \\ \frac{1}{L_{2a}} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} V_g \end{bmatrix}$$

Where

$A1_{11} = -\frac{r_{1a}}{L_{1a}}$, $A1_{22} = -[r_{1b} + r_{c1} + \frac{r_{o1}(R_L + r_{o2})}{R_L + r_{o2} + r_{o1}}](\frac{1}{L_{1b}})$,

$A1_{23} = -\frac{r_{c1}}{L_{1b}}$, $A1_{24} = -[r_{c1} + \frac{r_{o1}R_L}{R_L + r_{o2} + r_{o1}}](\frac{1}{L_{1b}})$, $A1_{25} = \frac{1}{L_{1b}}$,

$A1_{27} = [\frac{-(R_L + r_{o2})}{R_L + r_{o2} + r_{o1}}](\frac{1}{L_{1b}})$, $A1_{28} = [\frac{r_{o1}}{R_L + r_{o2} + r_{o1}}](\frac{1}{L_{1b}})$,

$$A1_{32} = -\frac{r_{c1}}{L_{2a}},\ A1_{33} = -\frac{(r_{2a} + r_{c1} + r_{c2})}{L_{2a}},\ A1_{34} = -\frac{r_{c1}}{L_{2a}},\ A1_{35} = \frac{1}{L_{2a}},$$
$$A1_{36} = -\frac{1}{L_{2a}},\ A1_{42} = -[r_{c1} + \frac{r_{o1}R_L}{R_L + r_{o2} + r_{o1}}](\frac{1}{L_{2b}}),\ A1_{43} = -\frac{r_{c1}}{L_{2b}},$$
$$A1_{44} = -[r_{2b} + r_{c1} + \frac{(r_{o1} + r_{o2})R_L}{R_L + r_{o2} + r_{o1}}](\frac{1}{L_{2b}}),\ A1_{45} = \frac{1}{L_{2b}},$$
$$A1_{47} = -[\frac{(R_L)}{R_L + r_{o2} + r_{o1}}](\frac{1}{L_{2b}}) = A1_{48},\ A1_{52} = -\frac{1}{C_1} = A1_{53} = A1_{54},$$
$$A1_{63} = \frac{1}{C_2},\quad A1_{72} = [\frac{R_L + r_{o2}}{R_L + r_{o2} + r_{o1}}](\frac{1}{C_{o1}}),$$
$$A1_{74} = [\frac{R_L}{R_L + r_{o2} + r_{o1}}](\frac{1}{C_{o1}}),$$
$$A1_{77} = [\frac{-1}{R_L + r_{o2} + r_{o1}}](\frac{1}{C_{o1}}) = A1_{78},$$
$$A1_{82} = -[\frac{r_{o1}}{R_L + r_{o2} + r_{o1}}](\frac{1}{C_{o2}}),$$
$$A1_{84} = [\frac{R_L}{R_L + r_{o2} + r_{o1}}](\frac{1}{C_{o2}}),\ A1_{87} = [\frac{-1}{R_L + r_{o2} + r_{o1}}](\frac{1}{C_{o2}}) = A1_{88},$$

The input current and output voltage are shown as output equations (C.10) and (C.11) as shown below.

$$i_g(t) = i_{1a}(t) + i_{2a}(t) \tag{C.10}$$

$$v_o(t) = -[\frac{r_{o1}R_L}{R_L + r_{o1} + r_{o2}} i_{1b}(t) + \frac{(r_{o1} + r_{o2})R_L}{R_L + r_{o1} + r_{o2}} i_{2b}(t) + \frac{R_L}{R_L + r_{o1} + r_{o2}} v_{o1}(t) + \frac{R_L}{R_L + r_{o1} + r_{o2}} v_{o2}(t)] \tag{C.11}$$

The output vector in matrix form is

$$\begin{bmatrix} i_g(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 & 0 & 0\,0 & 0 & 0 \\ 0\,C1_{22} & 0\,C1_{24} & 0\,0 & C1_{27} & C1_{28} \end{bmatrix} \begin{bmatrix} i_{1a}(t) \\ i_{1b}(t) \\ i_{2a}(t) \\ i_{2b}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{o1}(t) \\ v_{o2}(t) \end{bmatrix} + [0]$$

Where rows $i_g(t)$ and $v_o(t)$ are assigned respectively as $C_{mode1mR1}$ and $C_{mode1mR2}$, also $C1_{22} = -\dfrac{R_L * r_{o1}}{R_L + r_{o2} + r_{o1}}$, $C1_{24} = -\dfrac{R_L(r_{o2} + r_{o1})}{R_L + r_{o2} + r_{o1}}$, $C1_{27} = -\dfrac{R_L}{R_L + r_{o2} + r_{o1}} = C1_{28}$.

The state matrices in this mode are named as A_1, B_1 and C_1.

C.2 Mode 2 - S_1 and S_2 OFF $(t_1 - t_2)$

With rerence to the circuit diagram as shown in Fig.7.8, Modified ICC is modelled in Mode-2 is given as follows. The derivative of inductor current i_{1a} is given below as state equation (C.12) for inductor L_{1a}.

$$\frac{di_{1a}(t)}{dt} = -\frac{(r_{1a} + r_{c1})i_{1a}(t)}{L_{1a}} - \frac{v_{c1}(t)}{L_{1a}} + \frac{v_g(t)}{L_{1a}} \tag{C.12}$$

The state equation (C.13) gives differential of capacitor voltage of C_1.

$$\frac{dv_{c1}(t)}{dt} = \frac{i_{1a}(t)}{C_1} \tag{C.13}$$

The state equation for C_2 is given by (C.14)

$$\frac{dv_{c2}(t)}{dt} = \frac{i_{2a}(t)}{C_2} \tag{C.14}$$

The state equation for L_{2a} is given by (C.15)

$$\frac{di_{2a}(t)}{dt} = -\frac{(r_{2a} + r_{c2})}{L_{2a}} i_{2a}(t) - \frac{v_{c2}(t)}{L_{2a}} + \frac{v_g(t)}{L_{2a}} \tag{C.15}$$

Writing state equation for capacitor C_{o2} as shown in (C.16)

$$\frac{dv_{o2}(t)}{dt} = \frac{1}{(R_L + r_{o2} + r_{o1})C_{o2}}[-r_{o1}i_{1b}(t) + R_L i_{2b}(t) - v_{o1}(t) - v_{o2}(t)] \tag{C.16}$$

Writing state equation for Capacitor C_{o1} as shown in (C.17)

$$\frac{dv_{o1}(t)}{dt} = \frac{1}{(R_L + r_{o2} + r_{o1})C_{o1}}[(R_L + r_{o2})i_{1b}(t) + R_L i_{2b}(t) - v_{o1}(t) - v_{o2}(t)] \tag{C.17}$$

The state equation for L_{1b} is given by (C.18)

$$\frac{di_{1b}(t)}{dt} = -(r_{1b} + \frac{r_{o1}(R_L + r_{o2})}{(R_L + r_{o2} + r_{o1})})[\frac{i_{1b}(t)}{L_{1b}}] - \frac{r_{o1}R_L}{(R_L + r_{o2} + r_{o1})}[\frac{i_{2b}(t)}{L_{1b}}] - \frac{(R_L + r_{o2})}{(R_L + r_{o2} + r_{o1})}[\frac{v_{o1}(t)}{L_{1b}}] + \frac{r_{o1}}{(R_L + r_{o2} + r_{o1})}[\frac{v_{o2}(t)}{L_{1b}}] \tag{C.18}$$

The state equation for L_{2b} is given by (C.19)

$$\frac{di_{2b}(t)}{dt} = (-\frac{r_{o1}R_L}{(R_L + r_{o2} + r_{o1})})[\frac{i_{1b}(t)}{L_{2b}}] - (r_{2b} + \frac{(r_{o1} + r_{o2})R_L}{(R_L + r_{o2} + r_{o1})})[\frac{i_{2b}(t)}{L_{2b}}] - \frac{(R_L)}{(R_L + r_{o2} + r_{o1})}[\frac{v_{o1}(t)}{L_{2b}}] - \frac{R_L}{(R_L + r_{o2} + r_{o1})}[\frac{v_{o2}(t)}{L_{2b}}]$$

(C.19)

Writing the state equations (C.12), (C.18), (C.15), (C.19), (C.13), (C.14), (C.17) and (C.16) in matrix form

$$\begin{bmatrix} \frac{di_{1a}(t)}{dt} \\ \frac{di_{1b}(t)}{dt} \\ \frac{di_{2a}(t)}{dt} \\ \frac{di_{2b}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \\ \frac{dv_{o1}(t)}{dt} \\ \frac{dv_{o2}(t)}{dt} \end{bmatrix} = \begin{bmatrix} A2_{11} & 0 & 0 & 0 & A2_{15} & 0 & 0 & 0 \\ 0 & A2_{22} & 0 & A2_{24} & 0 & 0 & A2_{27} & A2_{28} \\ 0 & 0 & A2_{33} & 0 & 0 & A2_{36} & 0 & 0 \\ 0 & A2_{42} & 0 & A2_{44} & 0 & 0 & A2_{47} & A2_{48} \\ A2_{51} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & A2_{63} & 0 & 0 & 0 & 0 & 0 \\ 0 & A2_{72} & 0 & A2_{74} & 0 & 0 & A2_{77} & A2_{78} \\ 0 & A2_{82} & 0 & A2_{84} & 0 & 0 & A2_{87} & A2_{88} \end{bmatrix} \begin{bmatrix} i_{1a}(t) \\ i_{1b}(t) \\ i_{2a}(t) \\ i_{2b}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{o1}(t) \\ v_{o2}(t) \end{bmatrix}$$

$$+ \begin{bmatrix} \frac{1}{L_{1a}} \\ 0 \\ \frac{1}{L_{2a}} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} v_g(t) \end{bmatrix}$$

Where $A2_{11} = -\frac{(r_{1a} + r_{c1})}{L_{1a}}$, $A2_{15} = -\frac{1}{L_{1a}}$,

$A2_{22} = -[r_{1b} + \frac{r_{o1}(R_L + r_{o2})}{R_L + r_{o2} + r_{o1}}](\frac{1}{L_{1b}})$, $A2_{24} = -[\frac{r_{o1}R_L}{R_L + r_{o2} + r_{o1}}](\frac{1}{L_{1b}})$,

$A2_{27} = A1_{27}$, $A2_{28} = A1_{28}$, $A2_{33} = -\dfrac{(-r_{2a} - r_{C2})}{L_{2a}}$, $A2_{36} = A1_{36}$,
$A2_{42} = [-\dfrac{r_{o1}(R_L)}{R_L + r_{o2} + r_{o1}}](\dfrac{1}{L_{2b}})$, $A2_{44} = [-r_{2b} + \dfrac{-(r_{o1} + r_{o2})R_L}{R_L + r_{o2} + r_{o1}}](\dfrac{1}{L_{2b}})$,
$A2_{47} = A1_{47} = A2_{48}$, $A2_{51} = \dfrac{1}{C_1}$, $A2_{63} = A1_{63}$, $A2_{72} = A1_{72}$,
$A2_{74} = A1_{74}$, $A2_{77} = A2_{78} = A1_{77}$, $A2_{82} = A1_{82}$, $A2_{84} = A1_{84}$, $A2_{87} = A2_{88} = A1_{87}$.

The output vector is given by equations (C.20) and (C.21)

$$i_g(t) = i_{1a}(t) + i_{2a}(t) \tag{C.20}$$

$$\begin{aligned} v_o(t) = -[&\frac{r_{o1}R_L}{R_L + r_{o1} + r_{o2}} i_{1b}(t) + \frac{(r_{o1} + r_{o2})R_L}{R_L + r_{o1} + r_{o2}} i_{2b}(t) \\ &+ \frac{R_L}{R_L + r_{o1} + r_{o2}} v_{o1}(t) + \frac{R_L}{R_L + r_{o1} + r_{o2}} v_{o2}(t)] \end{aligned} \tag{C.21}$$

The output in matrix form is

$$\begin{bmatrix} i_g(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & C2_{22} & 0 & C2_{24} & 0 & 0 & C2_{27} & C2_{28} \end{bmatrix} \begin{bmatrix} i_{1a}(t) \\ i_{1b}(t) \\ i_{2a}(t) \\ i_{2b}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{o1}(t) \\ v_{o2}(t) \end{bmatrix} + \begin{bmatrix} 0 \end{bmatrix} \begin{bmatrix} v_g(t) \end{bmatrix}$$

Where rows $i_g(t)$ and $v_o(t)$ are assigned as $C_{mode2mR1}$ and $C_{mode2mR2}$ respectively. Where$C2_{22} = C1_{22}$, $C2_{24} = C1_{24}$, $C2_{27} = C2_{28} = C1_{27}$.

The state and output matrices in Mode-2 are termed as A_2, B_2 and C_2.

C.3 Mode 3 - S_1 OFF and S_2 ON $(t_2 - t_3)$

The state space model of Modified ICC based on the practical circuit diagram as shown in Fig.7.9 is given below.

The differential of current i_{1a} through inductor L_{1a} is given by the state equation (C.22)

$$\frac{di_{1a}(t)}{dt} = -\frac{(r_{1a} + r_{c1})i_{1a}(t)}{L_{1a}} - \frac{v_{c1}(t)}{L_{1a}} + \frac{v_g(t)}{L_{1a}} \tag{C.22}$$

The differential of voltage across C_1 is given by the state equation (C.23)

$$\frac{dv_{c1}(t)}{dt} = \frac{i_{1a}(t)}{C_1} \tag{C.23}$$

The derivative of voltage across C_2 is given by the state equation (C.24)

$$\frac{dv_{c2}(t)}{dt} = -\frac{i_{2b}(t)}{C_2} \tag{C.24}$$

The derivative of inductor current i_{2a} is given by the state equation (C.25)

$$\frac{di_{2a}(t)}{dt} = -\frac{r_{2a}}{L_{2a}} i_{2a}(t) + \frac{v_g(t)}{L_{2a}} \tag{C.25}$$

The differentila of voltage across capacitor C_{o2} is given by the state equation (C.26).

$$\frac{dv_{o2}(t)}{dt} = \frac{[-r_{o1}i_{1b}(t) + R_L i_{2b}(t) - v_{o1}(t) - v_{o2}(t)]}{(R_L + r_{o2} + r_{o1})C_{o2}} \tag{C.26}$$

The derivative of voltage across capacitor C_{o1} is given by the state equation (C.27)

$$\frac{dv_{o1}(t)}{dt} = \frac{[(R_L + r_{o2})i_{1b}(t) + R_L i_{2b}(t) - v_{o1}(t) - v_{o2}(t)]}{(R_L + r_{o2} + r_{o1})C_{o1}} \quad \text{(C.27)}$$

The voltage across L_{1b} is given by the equation

$$-r_{o1}C_{o1}\frac{dv_{o1}(t)}{dt} - v_{o1}(t) - r_{1b}i_{1b}(t) - L_{1b}\frac{di_{1b}(t)}{dt} = 0$$

Substituting equation (C.27) in the above expression, the current through L_{1b} is rewritten by the state equation (C.28).

$$\frac{di_{1b}(t)}{dt} = -(r_{1b} + \frac{r_{o1}(R_L + r_{o2})}{(R_L + r_{o2} + r_{o1})})[\frac{i_{1b}(t)}{L_{1b}}] - \frac{r_{o1}R_L}{(R_L + r_{o2} + r_{o1})})[\frac{i_{2b}(t)}{L_{1b}}]$$
$$-\frac{(R_L + r_{o2})}{(R_L + r_{o2} + r_{o1})}[\frac{v_{o1}(t)}{L_{1b}}] + \frac{r_{o1}}{(R_L + r_{o2} + r_{o1})}[\frac{v_{o2}(t)}{L_{1b}}] \quad \text{(C.28)}$$

Voltage across L_{2b} is given by the equation

$$-vo1(t) - r_{o1}C_{o1}\frac{dv_{o1}(t)}{dt} - r_{o2}C_{o2}\frac{dv_{o2}(t)}{dt} - v_{o2}(t) - r_{2b}i_{2b}(t)$$
$$-L_{2b}\frac{di_{2b}(t)}{dt} + r_{c2}i_{2b}(t) + v_{c2}(t) = 0$$

Substituting equations (C.26) and (C.27) in the above expression to obtain state equation (C.29) for L_{2b}.

$$\frac{di_{2b}(t)}{dt} = -\frac{r_{o1}R_L}{(R_L + r_{o2} + r_{o1})}[\frac{i_{1b}(t)}{L_{2b}}] + (-r_{2b} + r_{c2} - \frac{(r_{o1} + r_{o2})R_L}{(R_L + r_{o2} + r_{o1})})$$
$$[\frac{i_{2b}}{L_{2b}}] + \frac{v_{c2}(t)}{L_{2b}} - \frac{(R_L)}{(R_L + r_{o2} + r_{o1})}[\frac{v_{o1}(t)}{L_{2b}}] - \frac{R_L}{(R_L + r_{o2} + r_{o1})}[\frac{v_{o2}(t)}{L_{2b}}]$$

(C.29)

Writing the state equations (C.22), (C.28), (C.25), (C.29), (C.23), (C.24), (C.27) and (C.26) in matrix form

Writing the state equation in matrix form

$$\begin{bmatrix} \frac{di_{1a}(t)}{dt} \\ \frac{di_{1b}(t)}{dt} \\ \frac{di_{2a}(t)}{dt} \\ \frac{di_{2b}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \\ \frac{dv_{o1}(t)}{dt} \\ \frac{dv_{o2}(t)}{dt} \end{bmatrix} = \begin{bmatrix} A3_{11} & 0 & 0 & 0 & A3_{15} & 0 & 0 & 0 \\ 0 & A3_{22} & 0 & A3_{24} & 0 & 0 & A3_{27} & A3_{28} \\ 0 & 0 & A3_{33} & 0 & 0 & 0 & 0 & 0 \\ 0 & A3_{42} & 0 & A3_{44} & 0 & A3_{46} & A3_{47} & A3_{48} \\ A3_{51} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & A3_{64} & 0 & 0 & 0 & 0 \\ 0 & A3_{72} & 0 & A3_{74} & 0 & 0 & A3_{77} & A3_{78} \\ 0 & A3_{82} & 0 & A3_{84} & 0 & 0 & A3_{87} & A3_{88} \end{bmatrix} \begin{bmatrix} i_{1a}(t) \\ i_{1b}(t) \\ i_{2a}(t) \\ i_{2b}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{o1}(t) \\ v_{o2}(t) \end{bmatrix}$$

$$+ \begin{bmatrix} \frac{1}{L_{1a}} \\ 0 \\ \frac{1}{L_{2a}} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} v_g(t) \end{bmatrix}$$

Where
$A3_{11} = A2_{11}$, $A3_{15} = A2_{15}$, $A3_{22} = A2_{22}$ $A3_{24} = A2_{24}$,

$A3_{27} = A1_{27}$, $A3_{28} = A1_{28}$, $A3_{33} = \dfrac{-r_{2a}}{L_{2a}}$, $A3_{42} = A2_{42}$,
$A3_{44} = \dfrac{-r_{2b} - r_{c2}}{L_{2b}} - \dfrac{(r_{o1} + r_{o2})R_L}{(R_L + r_{o2} + r_{o1})L_{2b}}$, $A3_{46} = \dfrac{1}{L_{2b}}$,
$A3_{47} = A3_{48} = A1_{47}$, $A3_{51} = A2_{51}$, $A3_{64} = \dfrac{-1}{C_2}$, $A3_{72} = A1_{72}$,
$A3_{74} = A1_{74}$, $A3_{77} = A3_{78} = A1_{77}$, $A3_{82} = A1_{82}$, $A3_{84} = A1_{84}$,
$A3_{87} = A3_{88} = A1_{87}$.

The output is given by equations (C.30) and (C.31)

$$i_g(t) = i_{1a}(t) + i_{2a}(t) \tag{C.30}$$

$$\begin{aligned} v_o(t) = -[&\frac{r_{o1}R_L}{R_L + r_{o1} + r_{o2}} i_{1b}(t) + \frac{(r_{o1} + r_{o2})R_L}{R_L + r_{o1} + r_{o2}} i_{2b}(t) \\ &+ \frac{R_L}{R_L + r_{o1} + r_{o2}} v_{o1}(t) + \frac{R_L}{R_L + r_{o1} + r_{o2}} v_{o2}(t)] \end{aligned} \tag{C.31}$$

The output vector in matrix form is

$$\begin{bmatrix} i_g(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & C3_{22} & 0 & C3_{24} & 0 & 0 & C3_{27} & C3_{28} \end{bmatrix} \begin{bmatrix} i_{1a}(t) \\ i_{1b}(t) \\ i_{2a}(t) \\ i_{2b}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{o1}(t) \\ v_{o2}(t) \end{bmatrix} + \begin{bmatrix} 0 \end{bmatrix} \begin{bmatrix} v_g(t) \end{bmatrix}$$

Where rows $i_g(t)$ and $v_o(t)$ are assigned respectively as $C_{mode3mR1}$ and $C_{mode3mR2}$, $C3_{22} = C1_{22}$, $C3_{24} = C1_{24}$, $C3_{27} = C1_{27} = C3_{28}$.

The state and output matrices in Mode-3 are named as A_3, B_3 and C_3.

C.4 Mode 4 - S_1 and S_2 OFF $(t_3 - t_4)$

This mode is same as Mode-2. From the state space model, $i_g(t)$ and $v_o(t)$ are assigned respectively as $C_{mode4mR1}$ and $C_{mode4mR2}$, also the matrices are termed as A_4, B_4 and C_4.