# ANALYSIS AND DESIGN OF AN ADAPTIVE POLYNOMIAL PREDISTORTER WITH THE LOOP DELAY ESTIMATOR

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**ABSTRACT:** *Most adaptive linearization circuits for the nonlinear amplifier have a feedback loop that returns the output signal of the amplifier to the linearizer. The loop delay of the linearizer must be controlled precisely so that the convergence of the linearizer should be assured. In this Letter a delay control circuit is presented. It is a delay lock loop (DLL) with a modified early–late gate and can be easily applied to a DSP implementation. The proposed DLL circuit is applied to an adaptive linearizer with the use of a polynomial predistorter, and the simulation for a 16-QAM signal is performed. The simulation results show that the proposed DLL eliminates the delay between the reference input signal and the delayed feedback signal of the linearizing circuit perfectly, so that the predistorter polynomial coefficients converge into the optimum value and a high degree of linearization is achieved.*  Microwave Opt Technol Lett 34: 117–121, 2002: Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.10391

**Key words:** *adaptive linearization; loop delay estimator; DLL*

## 1. INTRODUCTION

Nowadays many communication systems adopt linear digital modulation schemes that have high spectral efficiency. These modulation schemes require the linearity of the communication system. To maintain high-quality communications services, it is very im-

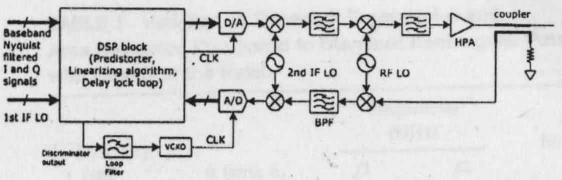


**Figure 1** Linear amplification system with the adaptive predistorter

portant to eliminate distortion of the transmitted signal. Therefore the nonlinearity of the power amplifier, which is a major contributor of nonlinearities in the transmitter, should be eliminated. Nonlinearity in a power amplifier generates in-band and out-of-band distortion by spectral regrowth, which causes the adjacent channel interference and degradation in the BER. Many linearization schemes, such as the backoff method, the LINC, the feedforward amplifier, the envelope elimination and restoration, the predistortion and the postdistortion are proposed [1–5]. Recently adaptive methods are widely used to keep the linearity regardless of ambient environments.

The structure of the adaptive linear power amplifier system necessarily has the part to compare the input signals of the linearizer to the feedback signals of the high power amplifier (HPA) output. The feedback signals of the HPA output are delayed a certain amount of time compared to the input signal of the linearizer. This delay must be eliminated so that the comparison of the feedback signal of the HPA output to the corresponding input of the linearizer can be performed in the same phase. To adjust this delay, the analog delay circuit that is affected by the ambient environments are typically used to delay the input signal of linearizer. To reduce the effect of the ambient environments, the loop delay estimator is proposed by Nagata [6] and Wright and Durtler [7]. The delay estimator proposed by Nagata is known to be lacking in accuracy, and the one by Wright and Durtler estimates the delay by FFT, which requires a tedious and time-consuming computation. In this Letter the DLL circuit that uses the modified early–late gate as the discriminator is proposed. The proposed DLL, which can easily be implemented in the DSP, is applied to the linearizer proposed by Ghaderi, Kumar, and Dodds [8].

The linearizer structure proposed by Ghaderi et al. has a polynomial-type predistorter that is appropriate to a DSP application because it has low memory requirements and simple numerical computations. But Ghaderi's work has the potential instability caused by the delay variations. A modified structure is presented and simulated. The simulated results show that the proposed DLL can compensate the delay between the linearizer reference input and the delayed feedback HPA output. The predistorter polynomial coefficients also converge and a high degree of linearization can be achieved.

## 2. STRUCTURE AND OPERATION OF THE POLYNOMIAL PREDISTORTER

Figure 1 shows the linear amplification system with an adaptive predistorter. In this system, the inputs of the DSP block are the digital-filtered baseband in-phase (I) and quadrature-phase (Q) signals and the first intermediate frequency (IF) local-oscillator (LO) signal. The DSP block includes the predistorter and the DLL discriminator to control the clock phase of the ADC (analog-to-digital converter) that samples the output of the HPA. In the DSP block, the baseband $I$ and $Q$ signals are predistorted and the predistorted signal is upconverted to the first IF band. Then the up-converted signal is applied to the DAC (digital-to-analog converter). It is converted to the second IF band and then to the RF